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GENERAL ANALYSIS OF VARACTOR FREQUENCY MULTIPLIERS WITH APPLICATION TO AN EXPONENTIAL C-V CHARACTERISTIC

by

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The undersigned certify that they have read, and recommend to the Faculty of Graduate Studies for acceptance, a thesis entitled "General Analysis of Varactor Frequency Multipliers with Application to an Exponential C-V Characteristic"
submitted by Wayne Ralph Tinga
in partial fulfilment of the requirements for the degree of Master of Science.

ABSTRACT

A critical review of varactor multiplier theory is given covering the more important analyses to date. Then a general analysis is presented for a N-times frequency multiplier in terms of the capacitance Fourier coefficients which can be derived for specific C-V characteristics. The analysis is based on the determination of the short circuit Y-parameters of a two-port where the varactor with ideal filters is regarded as the two-port network, and is series connected between the input and output ports. These Y-parameters are derived from the varactor equations of motion and by means of these the varactor multiplier behavior is completely specified. Application of this theory is then made to the case of a varactor with an exponential capacitance-voltage dependence such as occurs when a varactor is driven into the forward voltage region at high frequencies where the diode rectification mechanism fails. The necessary capacitance coefficients are solved for in terms of modified Bessel functions. Finally a set of theoretical curves of efficiency, load conductance, etc., versus frequency are given for a doubler and a tripler which indicate that "overdriving" a varactor is not detrimental to the efficiency of the multiplier but rather enhances it. Experimental proof of this efficiency increase has previously been reported in the literature but no theory was available which predicted this. Together with previously published analyses for reverse biased varactors this analysis specifies varactor behavior more completely under various operating conditions.

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LIST OF SYMBOLS

A_2	constant, $A_2 = \frac{k_2 e}{KT} = 30$ at room temperature
B_n	$B_n = A_2 Y_n$
$C(v)$	Voltage dependent diode capacitance.
C_m	Fourier capacitance coefficient at frequency $m\omega_o$
C_{min}	Minimum diode capacitance
C_{ov}	Capacitance at zero volts bias
G'	Shunt varactor loss conductance
G_c	Varactor conversion conductance
G_D	Parallel equivalent of series varactor loss resistance
G_{D_1}, G_{S_1}	Diode loss conductance at multiplier input frequency
G_{D_n}, G_{S_2}	Diode loss conductance at multiplier output frequency
G_g	Generator conductance
G_L, G_n	Multiplier Load conductance
I_k	Fourier coefficient of current at frequency $k\omega_o$
$I_p(Z)$	Pth order modified Bessel function of the first kind
M	$M = (C_{n-1} - C_{n+1})/C_{min} = \frac{M'}{2}$
$Q(v)$	Voltage dependent diode charge
R_s	Series varactor loss resistance
S_{max}	Maximum diode elastance
V	Applied diode voltage
V_{DC}	DC bias voltage

List of Symbols (Cont'd)

V_f	maximum forward diode voltage
V_{min}	minimum diode voltage
V_o	Normalization voltage: $V_o = V_f - V_{min}$
V_n	nth harmonic voltage
V_{B_D}	Diode breakdown voltage
X_n	Normalized conductance defined by $X_n = \frac{G_n}{G_{D_n}}$
Γ	Nonlinearity factor for reverse biased varactor diodes.
η	Multiplier efficiency
ϕ	Diode contact potential
ω_c	Varactor cutoff frequency: $\omega_c = \frac{1}{R_s C_{min}} = \frac{S_{max}}{R_s}$
ω_o	Multiplier input frequency

CHAPTER 1

INTRODUCTION

During the past few years the "State of the Art" of varactors has continually advanced with the result that highly efficient frequency multipliers are feasible at increasingly higher frequencies. Most varactors are normally operated over the reverse voltage region of the p-n junction and their behavior in this region is well known and good design theories have been presented. However, many researchers have indicated that when the varactor is "overdriven" under high power input conditions or by the use of "self-bias" its behavior is affected by what happens when the large voltage swing carries the diode into the forward voltage region. At high frequencies the rectification mechanism, usually present in diodes for positive voltages, fails due to the finite recombination time of the current carriers in the semiconductor material. It has been indicated in many cases that the varactor capacitance-voltage dependence becomes exponential under these conditions and the diode acts as a fairly low loss capacitor capable of storing a very large amount of charge. No theory as to the behavior of multipliers using such an exponential characteristic has been given in the literature. The charge storage effect has been treated to some extent by various authors, but an ideal capacitance-voltage curve was assumed in all cases, i.e., zero capacitance under reverse bias and infinite capacitance for positive bias. They have assumed that the reverse bias region contributes nothing to the multiplier efficiency which

is not a valid assumption since efficiencies of multiplication can be very high when operating only in the reverse bias state. Several authors have indicated that an increase in efficiency results when the diode is driven positive but no theory was available to predict this. An exact analysis would require the consideration of both reverse bias and forward bias harmonic generation simultaneously. This problem, unfortunately, is a very untractable one. If now one would carry out an analysis separately for the forward bias case a good evaluation of the result of "overdriving" could be obtained with respect to an increase or decrease in efficiency of multiplication. Moreover, an analysis for an exponential C-V characteristic could be used in determining the efficiency of harmonic generation for surface varactors since they exhibit such a characteristic also.

This thesis solves the problem of large signal harmonic generation for such a highly nonlinear device. In order to achieve this a general theory is presented in chapter three for an N×-multiplier in which the varactor is series connected between the input and output ports of the network. For the case of an exponential capacitance behavior, the necessary Fourier capacitance coefficients are solved in chapter four using modified Bessel functions; and a set of curves relating optimum multiplier efficiency and load conductance to the normalized input frequency is given in chapter five. These curves are independent of the varactor used. The evaluation of optimum values requires a certain optimization procedure

which is discussed in chapter five. The theory presented might also be applied to tunnel diode devices which exhibit exponential nonlinearities. Moreover, a review of the history of varactor multipliers is given in chapter two with various comments on the past work in the light of present day knowledge about the subject.

CHAPTER 2

CRITICAL REVIEW OF VARACTOR DIODE THEORY AND FREQUENCY MULTIPLIERS

In this chapter a qualitative review of the varactor multiplier theory will be given and an evaluation in terms of the present knowledge about the subject will be made. Not all the history and facts on this subject can be given but a fairly comprehensive discussion of the major aspects will be presented.

2.1 - Varactor Diode Characteristics

In this section the capacitance-voltage and charge-voltage curves will be described as well as other physical diode characteristics of various types of varactors as classified by their actual capacitance-voltage dependence.

2.1.1 - Abrupt Junction or Square Law Varactor

The type of varactor where the diode capacitance is inversely proportional to the square root of the diode voltage is commonly called the abrupt junction varactor. The abrupt p-n junction has constant resistivity near the depletion region (see figure 1)⑤ and the doping on each side of the junction is independent of x (see figure 2) in the reverse biased state.②

This leads to the following dependence of junction capacitance on voltage:

$$C = C_{min} \left(\frac{V_{BD} + \phi}{v + \phi} \right)^{\frac{1}{2}} \quad \text{or} \quad S = S_{max} \left(\frac{v + \phi}{V_{BD} + \phi} \right)^{\frac{1}{2}}$$

Where C_{min} is the junction capacitance at the breakdown voltage V_{BD}; v is the applied voltage, including the negative bias, and is measured as positive in the increasing negative direction; ϕ is approximately equal to the contact potential of the p-n junction and is a small positive voltage; $S_{max} = 1/C_{min}$, the maximum elastance, again measured at the breakdown voltage.

These formulas are valid only for $V_{BD} \geqslant v > -\phi$

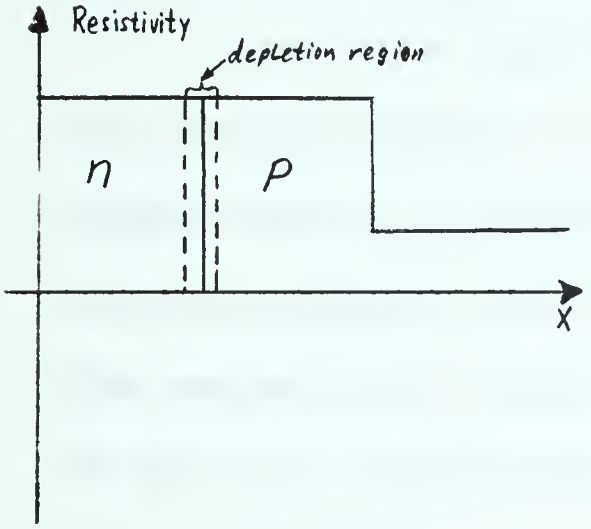


Fig. 1 Resistivity Profile of an Abrupt p-n Junction

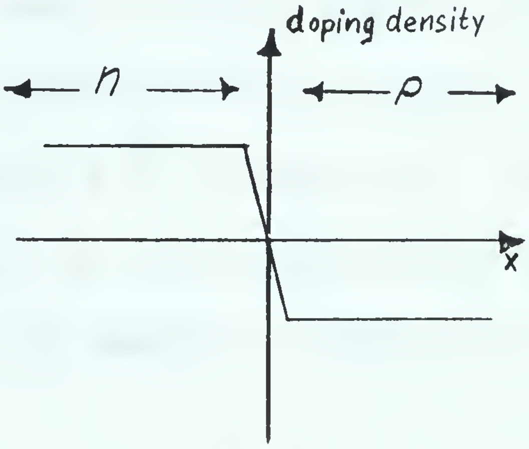


Fig. 2 Doping Density of an Abrupt p-n Junction

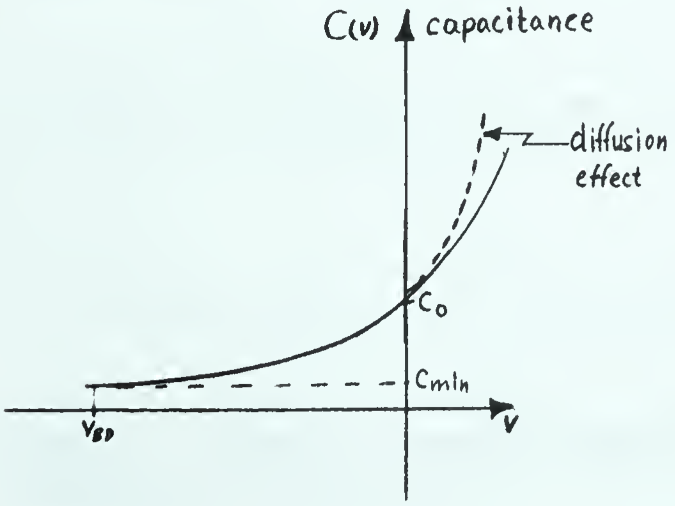


Fig. 3 C-V Characteristic of an Abrupt Junction Varactor

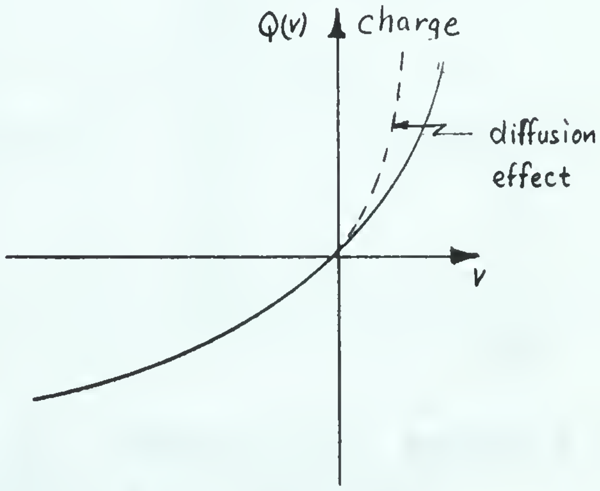


Fig. 4 Q-V Characteristic of an Abrupt Junction Varactor

A qualitative capacitance-voltage curve is given in figure 3 and figure 4 shows the relationship between charge and voltage. The dotted portion of the curves (figures 3 and 4) is the effect of reactive diffusion current flowing under forward bias. ③ In the forward voltage region the capacitance increases exponentially with voltage. This effect is also called charge storage⑤ and occurs over a limited but quite wide frequency range.

2.1.2 - Graded Junction Varactor (1/3 "power" law)

For this junction the diode capacitance is inversely proportional to the cube root of the applied voltage. Graded junction devices have a doping density which varies linearly with the distance x ② (figure 5). Since the resistivity varies inversely as the impurity level, we get the resistivity profile as shown in figure 6.

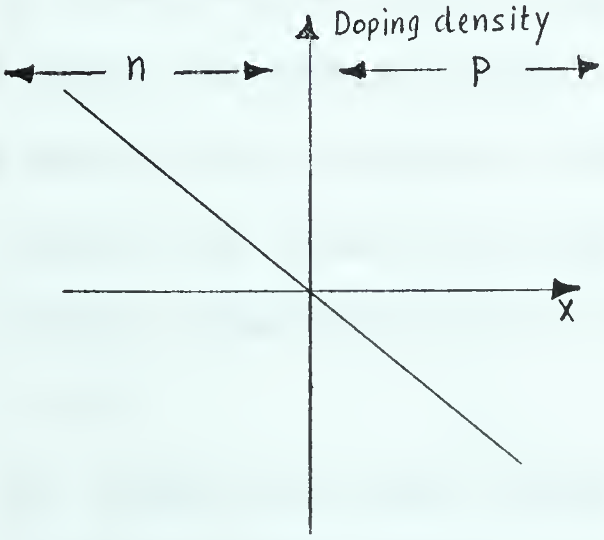


Fig. 5 Doping Density of a Graded p-n Junction

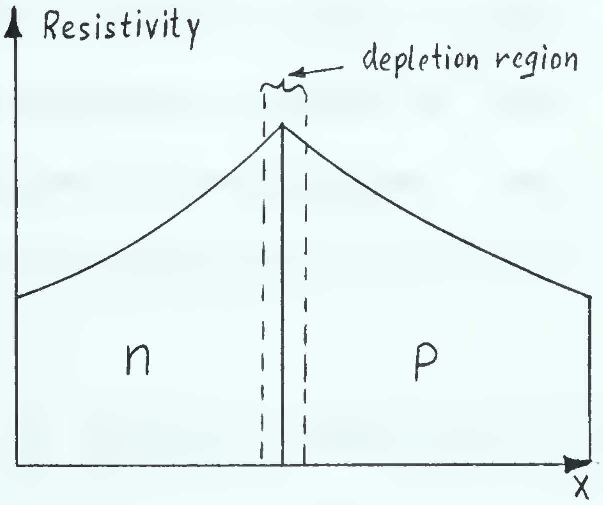


Fig. 6 Resistivity Profile of a Graded p-n Junction

This linearly doped junction gives rise to the following capacitance-voltage relationship:

$$C = C_{min}\left(\frac{V_{BD} + \phi}{V + \phi}\right)^{1/3}$$

or

$$S = S_{max}\left(\frac{V + \phi}{V_{BD} + \phi}\right)^{1/3}$$

with the definitions of the terms the same as in section 2.1.1.

Thus the capacitance voltage and charge voltage curves are very similar to those given in figure 3 and figure 4, the only difference being that the capacitance and charge change less rapidly with voltage in the reverse biased state. However, in the forward region the diffusion current effect is more pronounced (i.e., a steeper increase of capacitance with voltage) in graded junctions than in abrupt junctions. This is due to the higher resistivity peaking near the depletion layer.
In other words, this high resistivity gives rise to higher retarding fields and thus charge tends to stay close to the junction boundary and thus there is less chance for these minority carriers to recombine. For further remarks on this effect see sections 2.1.3 and 2.1.4.
The depletion layer width is, of course, dependent on the applied diode voltage.

2.1.3 - Special Diffused Junction Varactor (1/5 power law)

Diffused junction diodes are very similar to graded junction devices since both exhibit the favorable characteristics of charge storage and low series resistance.

However, the special diffused junction, reported by G. Schaffner ⑤, has a greater change of resistivity near the depletion region and for this reason charge storage (of minority carriers) occurs very close to the junction, reducing recombination of the minority carriers and increasing the speed of step recovery as in step diodes.

The doping density as a function of x and the resistivity as a function of x are displayed in figure 7 and figure 8 respectively.

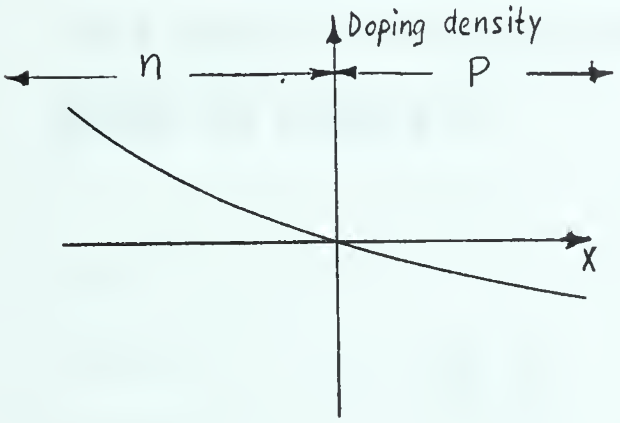


Fig. 7 Doping Density of a Diffused p-n Junction

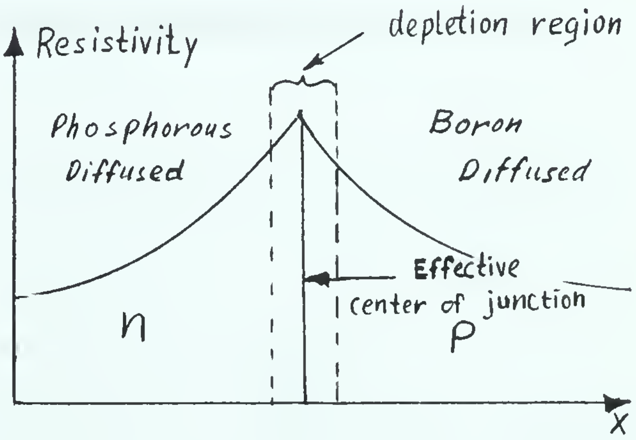


Fig. 8 Resistivity Profile of a Phosphorus-Boron Diffused p-n Junction

It is the resistivity profile of figure 8 which leads to certain advantages of the special diffused junction over the linearly graded junction.

A direct result of the steep resistivity gradient near the depletion layer is high breakdown voltage since

it depends on the resistivity of the active semiconductor region. Further, large power handling capability of the junction is an expected natural result since power is proportional to V_{BD}^2 for the graded and abrupt junctions where V_{BD} is the breakdown voltage.

Moreover, charge storage is enhanced in this diode since the high retarding fields built into the junction keep the stored charge close to the depletion region. (Also see section 2.1.4).

The resistivity of figure 8 leads to the following expression for junction capacitance under reverse bias: ⑤

$$C = C_{min} \left(\frac{V_{BD} + \phi}{V + \phi} \right)^{1/5}$$

with definitions as in section 2.1.1.

This gives the capacitance-voltage characteristic as shown in figure 9.

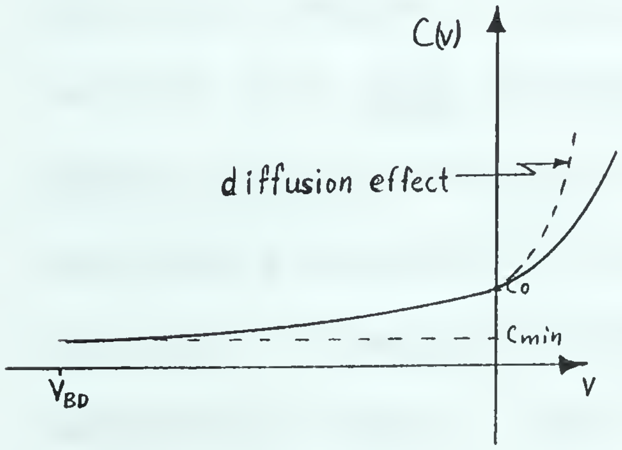


Fig. 9 C-V Characteristic of a Special Diffused Varactor

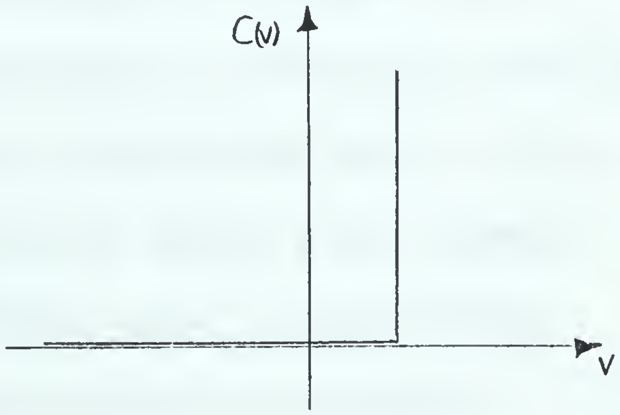


Fig. 10 C-V Characteristic of an Ideal Diode

As before, the dotted portion of the curve in figure 9 indicates the effect of driving the diode into the forward voltage region and generating reactive diffusion current. This diode more closely approximates an ideal diode, figure 10, than either the abrupt or linearly graded devices.

As already mentioned, the high resistivity in the depletion layer gives rise to a high breakdown voltage but high resistivity also increases the series resistance of the diode which leads to poor efficiency in frequency multipliers. However, the fact that the resistivity peaks so sharply at the semiconductor junction indicates that the resistivity falls off very rapidly as we move away from the actual junction. The following argument will show how high breakdown voltage and low series resistance can be compatible in this special diffused diode.

To oppose the effects of an applied voltage a fixed amount of charge must be included within the depletion region. Since this depletion layer is located in a high resistivity region, and since the fixed charge density is less in high resistance than in low resistance material, the depletion layer will spread rapidly to take up a considerable part of this high resistance region. Now, we know that the series resistance is calculated by integration of the resistivity over the path of the current. Furthermore, it is a fact

that when charge is supplied to the junction it travels only to the edge of the depletion layer. Thus the current path only includes the low resistivity ends of the semiconductor. For now the high resistivity region is part of the depletion layer. So one would also expect the series resistance to decrease with increasing reverse voltage. Further one would expect the incremental change in capacitance to decrease in magnitude as the voltage is increased. This is because the depletion layer spreads considerably after the application of an initially low voltage and any further increase in voltage has only a small effect. (Think of the analogy with capacitor plates). These variations indeed do occur in the special diffused diode.

2.1.4 - Surface Varactors and the Exponential Capacitance-Voltage Dependence in p-n Junctions Under Forward Bias.

There is still another type of varactor called the "Surface varactor". ⑦ ⑧ Unlike the other types it consists of a layer of metal, oxide, and semiconductor material respectively (see figure 11). When the oxide is positive a so-called "accumulation" layer is formed and the capacitance increases as exp (eV/KT) and with the oxide slightly negative a depletion layer results for which the capacitance varies as $V^{-\frac{1}{2}}$. At higher negative voltages an inversion layer is formed for which the capacitance increases as exp (-eV/KT), where V now is a negative voltage (see figure 12).

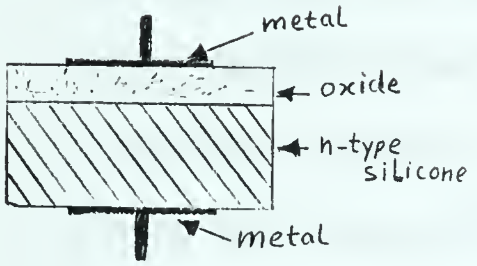


Fig. 11 Surface Varactor - ON - type Structure

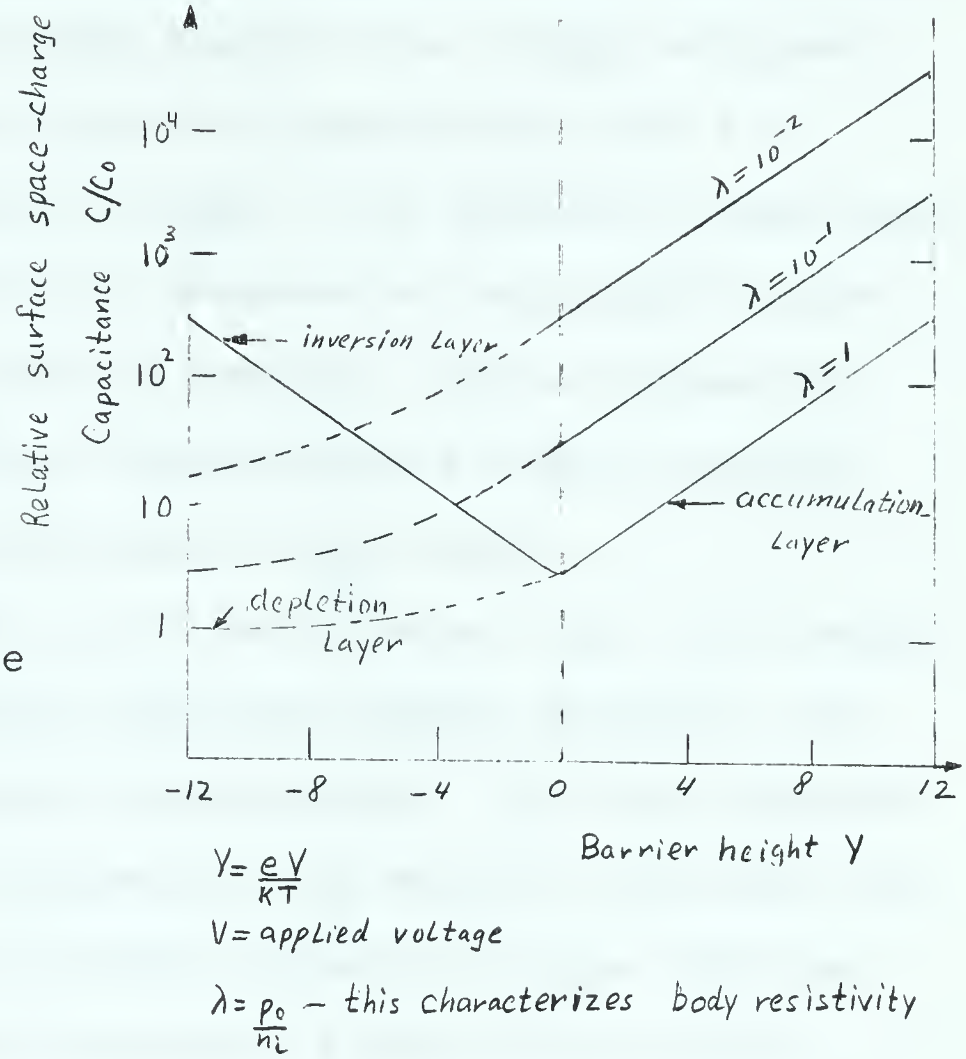


Fig. 12 C-V Characteristic of a Surface Varactor

If now the oxide has a small value of conductance, (of the order of that of a reverse biased p-n junction) the inversion layer won't form and the device will exhibit the depletion layer capacitance (dotted curves) for large negative values of V (i.e. for $|V| > KT/e$).

The direct consequence for harmonic generation is that at voltages which drive the device slightly into the forward region a large increase in device capacitance results which gives rise to a higher harmonic content of the output wave.

Secondly, we will consider the exponential capacitance-voltage dependence of p-n junctions.

According to Leeson ① the diffusion current which flows in a p-n junction under forward bias (large compared to KT/e) is mainly reactive (capacitive) over a considerable frequency range. The diffusion capacitance under these conditions increases as exp (eV/KT) where V is the applied forward voltage. By the arguments given by Leeson ③ one would expect a higher harmonic content in the output wave of the diode.

Furthermore, C.T. Sah (19) shows that for forward bias voltages greater than the contact potential the capacitance increases exponentially. He also observes that for longer lifetimes of the minority carriers this behavior extends to higher forward voltages than for diodes with lower lifetimes. A qualitative graph showing this is given in figure 13. Moll, et all, ⑥ shows that the stored charge or capacitance varies in the forward bias direction as exp $\left(\frac{3}{4}\frac{eV}{KT}\right)$.

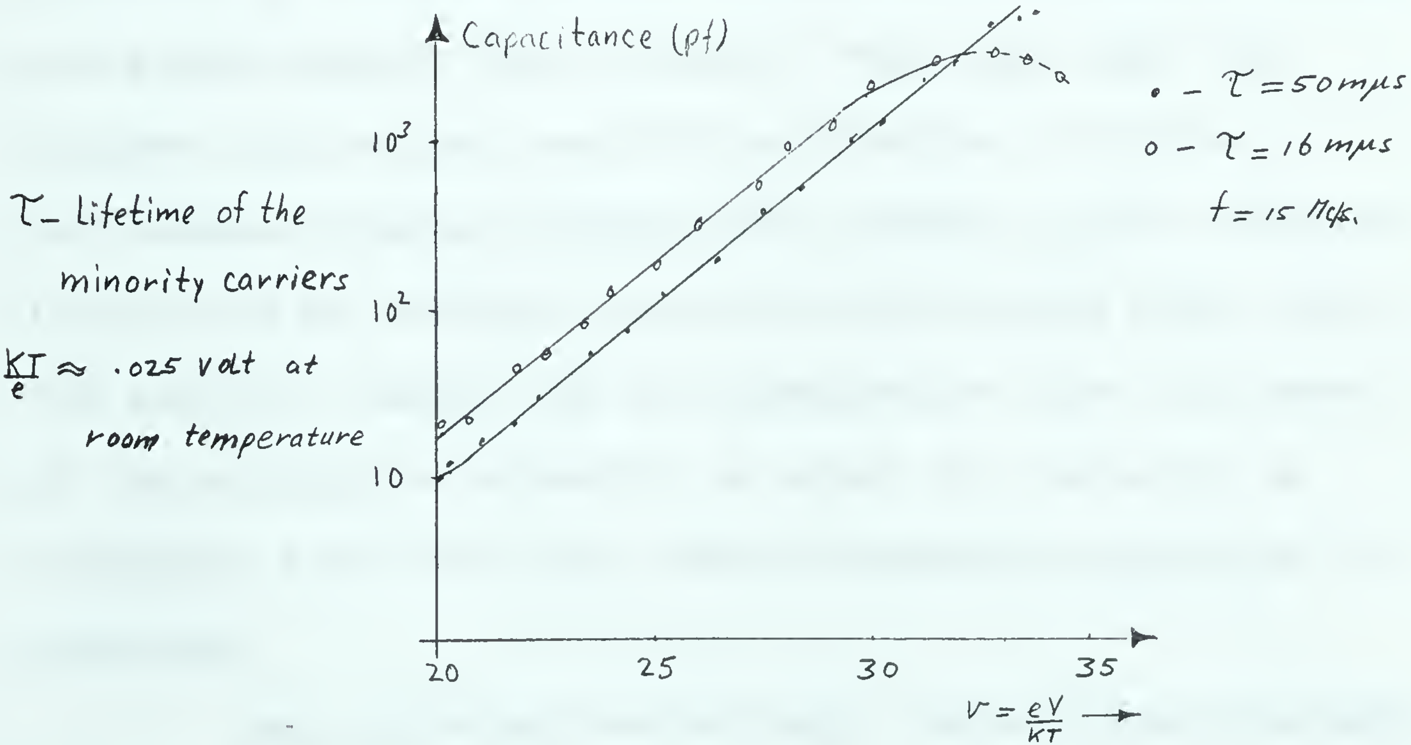


Fig 13. C-V Characteristic of a Forward Biased p-n Junction Varactor

2.2 - Methods of Analysis for the Various Varactors

This section will be devoted to a qualitative discussion on the methods of analysis used for the different types of varactors. Only the more useful and important analyses reported in the literature will be covered. Many small signal analyses done in the early stages of the Varactor multiplier history will be omitted since they have been replaced in recent years by more practical large signal theories.

2.2.1 - Abrupt Junction Varactor ($\frac{1}{2}$ power law)

2.2.1.1 By far the best and most useful analysis for this varactor is given by B.L. Diamond ④ and Penfield and Rafuse ②. They consider the varactor as charge-or current-controlled using the fact that for the abrupt-junction varactor the charge is proportional to the elastance in the reverse-biased region. (N.B. In all the following examples the theory applies only when the varactor is driven between the reverse breakdown voltage and approximately zero volts.). They also take into account the series loss of the varactor. All the performance limits obtained are related to the varactor itself and no external circuit restrictions enter into the analysis except for the assumptions that all parts of the multiplier circuit, in which the varactor is imbedded, are tuned and ideal frequency separation is required.

By expanding the voltage, current, and elastance

variables in complex Fourier series the voltage coefficients are related to the current and elastance coefficients. Knowing that the current coefficients are proportional to the elastance coefficents (for the abrupt junction varactor only) the voltages are completely specified in terms of the normalized elastance coefficients. B.L. Diamond also establishes the idler requirement which states that for an abrupt junction varactor to generate frequencies at other than twice the input frequency, there must be idler or intermediate frequency currents flowing through the varactor. This results from the fact that the abrupt junction diode is a square law device when reverse biased. The normalized elastance is shown to have an average value which depends upon the bias conditions and the magnitude of the applied R-F drive, and a varying component which is an odd function of time.

All the operating variables of the varactor multiplier depend on the input drive level. Diamond has solved the resulting highly complex algebraic equations by means of iterative techniques on a digital computer, obtaining many useful graphs which display the important multiplier parameters as functions of frequency. Some of these theoretical results are reproduced in section 2.3.1.

2.2.1.2 Another fairly extensive analysis has been carried out by T. Utsunomiya and S. Yuan ⑪. Their results are similar to those obtained by Diamond. They

analyze only one particular multiplier with idlers, namely, a quintupler.

Using a Taylor series expansion of the capacitance characteristic and a Fourier expansion of the voltage and charge variables they show that for the abrupt junction varactor only the first three terms (including the D.C. term) of the Taylor series are nonzero. Like B.L. Diamond they use the tuning condition on input, output, and idler ports. Their analysis, however, is developed in terms of circuit Q-factors, and it is for that reason not apparent how the actual diode characteristics effect the efficiency, power output, etc., of the multiplier. The authors work with a set of equivalent circuits which are deduced from the charge-voltage relationships of the varactor. These are in agreement with those derived in a later paper by H.L. Kaylie ⑮ who gives equivalent multiplier circuits based on the theory of B.L. Diamond ④. Utsunomyia and Yuan further assert that stray diode capacitance affects the conversion efficiency, and proceed to calculate this effect. They say that the nonlinearity, Γ,

$$\text{(from } C(v) = \left(\frac{V_B + \varnothing}{V + \varnothing}\right)^{-\Gamma} \quad \text{where } 1 \geqslant \Gamma \geqslant 0)$$

of the diode is reduced by stray capacitance across the actual variable capacitance. This assumption is in error since the stray capacitance just adds a constant to the diode characteristic and does not affect the nonlinearity at all. It does, however, change the impedance level of the multiplier.

2.2.1.3 - A much more practical, although not as rigorous,

approach to the abrupt junction varactor frequency multiplier is given in reference 13. Here the authors assume certain sinusoidal current components to exist on the varactor (i.e., only certain frequencies are permitted to exist in the multiplier circuit by the use of ideal filters). They substitute the corresponding expression for charge directly into the equation which relates voltage to charge and expand the result by the use of trigonometric identities. Thus they obtain various frequency components of voltage in terms of the various current magnitudes, the average diode capacitance, and the frequency. Interpreting these different terms with respect to power sources or sinks they arrive at various conditions on the current magnitudes and phase angles and so obtain efficiency and power relations in terms of the multiplier variables.

They neglect losses in the derivation of their relations but later discuss them and evaluate their effect on device operation. Moreover, they give a helpful procedure for designing practical frequency multiplier circuits (see also section 2.4.1).

Generally their discussion brings to light the actual mechanism of power transfer and presents the whole problem of frequency multiplication in a more physically meaningful way. Their theoretical analysis, however, is used only as an initial design step. Some circuit modifications are then indicated which give highly improved performance.

2.2.1.4. An analysis quite different from the previous ones was carried out for the abrupt junction varactor by

K.K.N. Chang ⑰. The analysis is done in essence, by an iterative procedure. First a set of trial input and output voltages is assumed to drive the varactor diode. Then the nonlinear charges which appear on the diode are Fourier analyzed by use of the proper charge-voltage relations. From these the desired fundamental and harmonic components are obtained which must satisfy a particular circuit configuration (defined by the available input power, the diode bias voltage and the circuit Q's). The reaction of the circuit will now result in another set of input and output voltages on the varactor which may be different from the original trial values. The computations are then cyclically repeated until the two sets of voltages are equal and consistent. These voltages are then the correct solutions. This type of analysis can be applied to any nonlinear reactance device and is thus quite general. Unfortunately, the treatment is quite brief and his results are not easily checked against those of earlier papers. A quick substitution, however, of variables in his (17-21) give

$$\eta = \frac{G_c\ G_L}{(G_{s1} + G_c)\ (G_L + G_{s2})}$$

where G_{s1} and G_{s2} are the loss conductances in the input and output circuit respectively (G_c being the conversion conductance and G_L the load conductance). This checks with the efficiency calculated from figures 5 and 6 of Johnson ⑫. Chang's efficiency and power output curves are not very useful for design purposes.

2.2.2 - Graded Junction Varactor (1/3 power law)

2.2.2.1 The analysis by M. Greenspan referred to in appendix F of reference 2 applies to graded junction varactor multipliers and is also a very thorough analysis of a graded junction doubler. Assuming only two frequency components of current to exist in the circuit the normalized charge components are obtained which obey the restriction that the charge must lie between the charge at the breakdown voltage and the contact potential. (Note: It is suggested by the author of this thesis that the minimum voltage should be zero rather than the small forward contact potential since even for small forward voltages the capacitance law which Greenspan assumes is no longer valid).

Furthermore Greenspan proceeds to calculate the Fourier elastance and voltage coefficients but it is not indicated in the abbreviated version of Greenspan's analysis ② by what procedure the author does this. However, since the total charge on the varactor is physically restricted to lie between a definite upper and lower limit, using this condition one can presumably obtain the voltage Fourier coefficients for bias, input, and output voltage. The other necessary parameters such as $Z_{in} = V_1/I_1$ can then be calculated where Z_{in} is, in general for all multipliers, a function of drive level. Taking real and imaginary parts of this equation one can obtain the input resistance which then makes possible the

determination of the multiplier efficiency given by

$$\eta = \frac{R_{in} - R_s}{R_{in}} \quad \frac{R_2}{R_2 + R_s}$$

where R_{in} = input resistance

R_s = series varactor loss resistance

R_2 = output load resistance.

Again, the tuning assumption is made that the input and output currents are in phase with the realization that a higher efficiency may be possible with a slight detuning of the multiplier.

The efficiency of the graded junction varactor doubler is very close to the maximum efficiency of the abrupt junction device as analyzed by B.L. Diamond ④.

It is interesting to note that for the graded junction varactor the imaginary parts of Z_{in} and Z_{out} of the device are no longer equal to the reactance of the average elastance S_o or capacitance C_o at the respective frequencies. This means that to tune the multiplier input, output, and idler ports (for graded junction devices) we must calculate these reactances from the ratios: V_1/I_1, V_k/I_k, and V_n/I_n, which generally are complex. (k refers to idler frequency, and n to the output frequency). Greenspan further gives asymptotic formulas for the low and high frequency cases.

2.2.2.2 A more general approach is used by K. Johnson ⑫ which applies to both abrupt and graded junctions since he does not specify the nonlinearity factor, Γ, of the diode. He works out a large-signal solution for an n-times

multiplier. First, he converts the normally used series model for the varactor to the parallel equivalent which makes the new parallel loss conductance frequency dependent: $G_D = \omega^2 C_{min}^2 R_s$, where R_s is the original series resistance of the varactor, C_{min} is the minimum diode capacitance and ω is the input or output frequency. This is a simplified expression for G when the Q of the diode is large (i.e., R_s is small) and the operating frequency is reasonably high. Assuming a voltage to exist on the diode which has a D.C., fundamental, and an n^{th} harmonic cosine term, he then writes the charge in terms of a Fourier series. As an approximation he indicates that for large harmonic numbers, n, the output voltage becomes very small compared to the input voltage and the charge coefficients can then be evaluated by means of a hypergeometric series which converges very rapidly. (This procedure is also used in reference (2) and (14) for application to parametric devices). For the large-signal case where V_n, the output voltage, is not negligible, Johnson uses numerical integration techniques for evaluating the charge coefficients. However, the remarks made on a special integration technique he uses are rather vague.

2.2.3 - Special Diffused Junction Varactor (1/5 power law and charge Storage Effects)

Recently, G. Schaffner ⑤ reported a new high-power varactor of the diffused type. The paper gives a qualitative discussion of the diode and associated

multiplier circuitry. Under reverse bias conditions the diode's depletion layer capacitance is inversely proportional to the fifth root of the applied voltage, whereas under forward applied voltage the so-called charge storage effect exists to a very high degree. Schaffner discusses the diode mainly with regard to this charge storage effect and assumes that little harmonic generation occurs in the reverse biased region.

Some results on the harmonic content of the resultant current wave form are presented in his paper. The author Fourier analyzes an impirically determined current waveform and plots its harmonic content (second, third, and ninth harmonic) as a function of the rise time ($\Delta\alpha$) of the recovery step. His diagram is reproduced in figure 14.

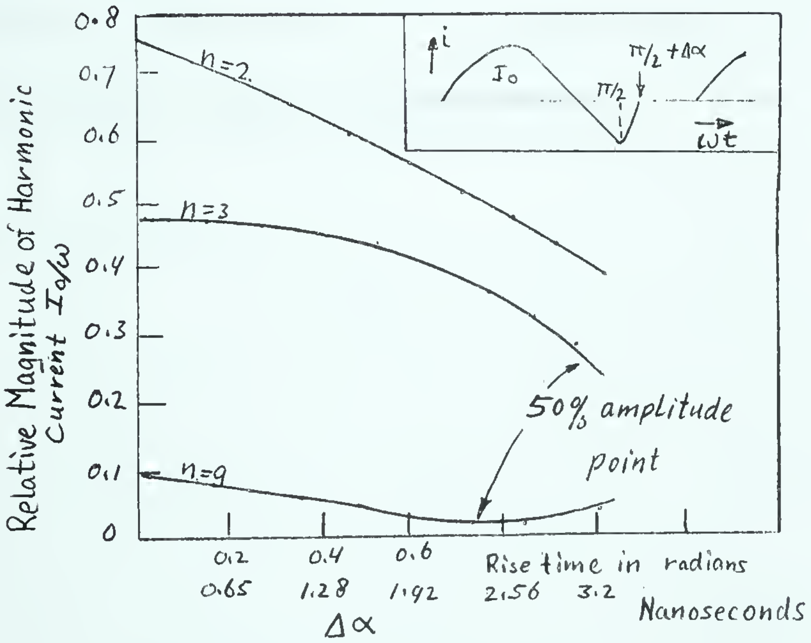


Fig. 14 Harmonic Current of Step-Recovery Diode

"Relative harmonic amplitude is shown as a function of the rise time $\Delta\alpha$ of the recovery step. Faster recovery corresponds to greater percentage of harmonic current. In the upper right hand corner is the current waveform of a step-recovery diode."

Experimental efficiencies of the order of 70% are reported by this author as well as a tremendous increase in power handling capability over previous varactors. For further discussion on his results and circuits see sections 2.3.3 and 2.3.4.

A future detailed analytic investigation of the performance of this specific diode may be worthwhile, to see whether the effect of the reverse biased region is really as slight as assumed here.

2.2.4 - Surface Varactors and the Exponential Capacitance Voltage Dependence in p-n Junctions under Forward Bias

The capacitance-voltage law for these devices is exponential in nature under certain operating conditions (see section 2.1.4). No analysis has as yet been reported for this exponential capacitance-voltage variation. The latter part of this thesis deals specifically with this problem and a large signal analysis for this case is presented.

2.3 - Important Theoretical and Experimental Results for Various Multiplier Characteristics

The results given in this section will be mainly those reported by previously mentioned authors.

2.3.1 - Abrupt Junction Varactor Multiplier

Undoubtedly the characteristic of the most interest is the efficiency of multiplication and the manner in which it varies with multiplier input or output frequency. An attempt will be made to compare the results of different authors for similar devices.

First a few of B.L. Diamond's ④ results are given, assuming no losses in any of the idling (or intermediate frequency) circuits. See figures 15, 16, 17, and 18. The diagrams are self explanatory. Diamond has not given any experimental curves for comparison. However, the predicted high efficiencies have been verified by many researchers working with these devices. Of course, circuit losses can be accounted for by lumping them with the input, output, and idler resistances.

Utsonomyia and Yuan ⑪ give some theoretical and experimental results for an abrupt-junction varactor quintupler (see figure 19). The frequency dependence of the efficiency is not discussed at all in this paper which is rather unfortunate since it is such an important factor in harmonic frequency multipliers. The curves follow the general pattern of that indicated by Diamond (compare figure 18 with figure 19) but it is hard

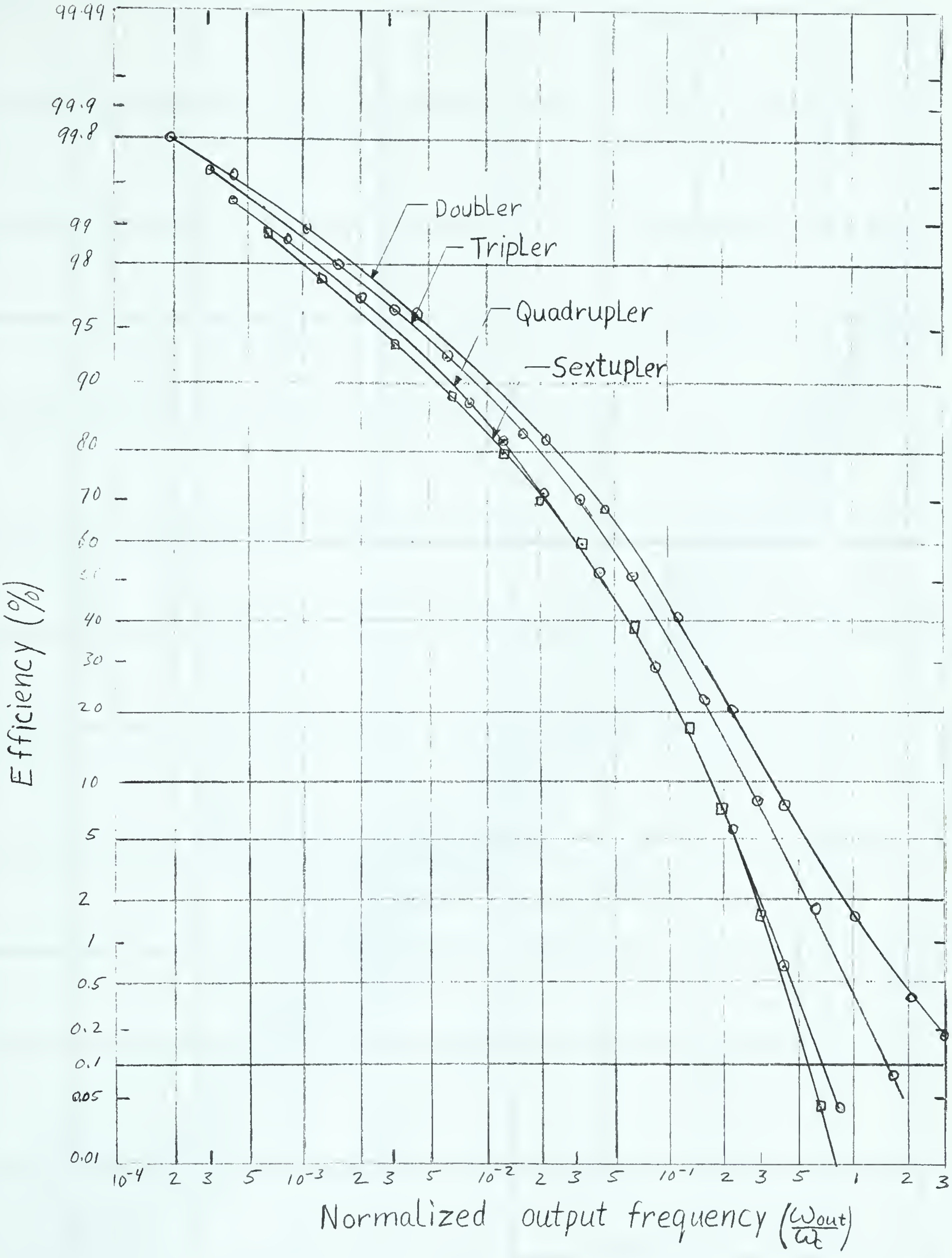


Fig. 15 Efficiency versus Frequency for Abrupt Junction Varactor Multipliers with the Idlers Assumed Lossless.

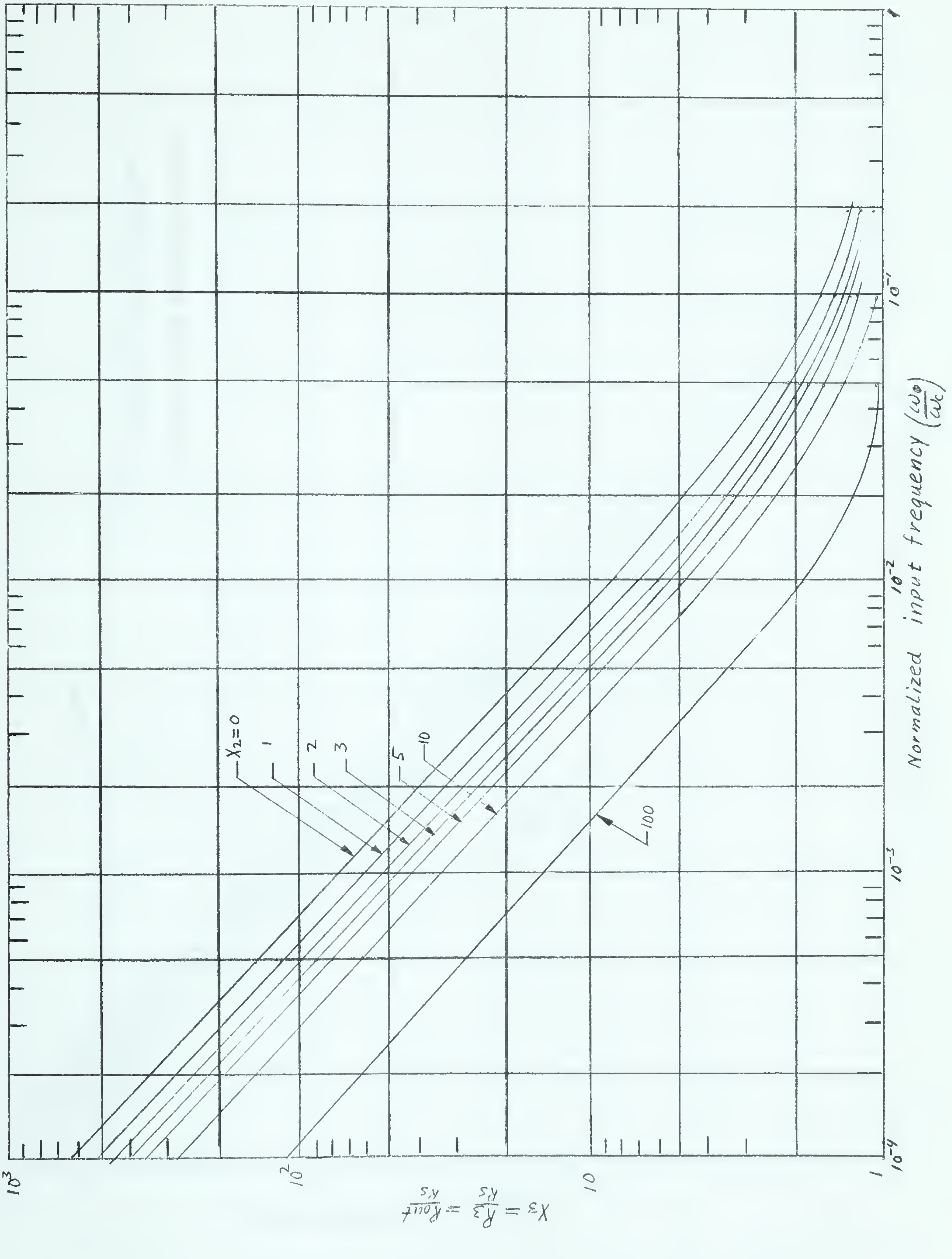


Fig. 16 Load Resistance versus Frequency for Abrupt Junction Varactor Tripler with Idler Resistance as a Parameter and Idler at $2\omega_0$.

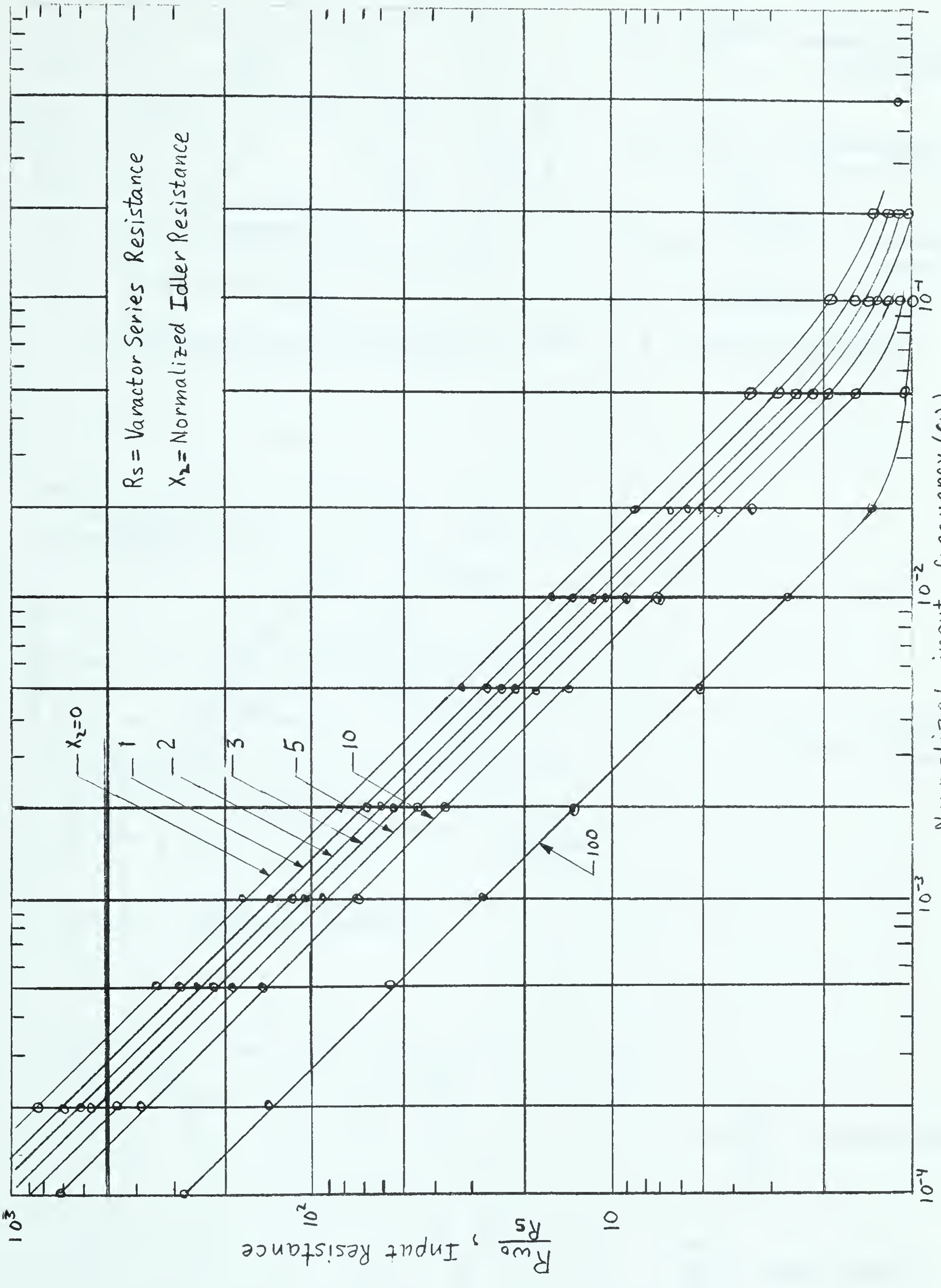
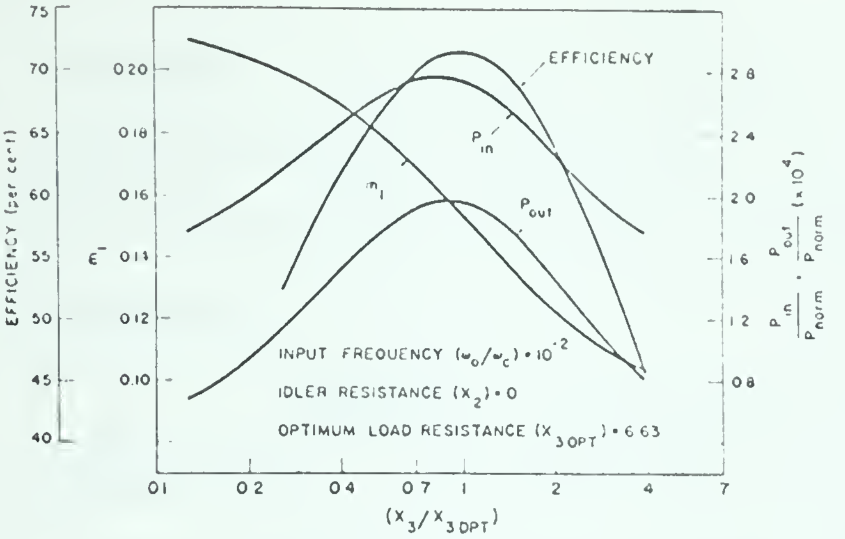


Fig. 17 Input Resistance versus Frequency for Abrupt Junction Varactor Tripler with Idler Resistance as a Parameter and Idler at $2\omega_0$.



Typical performance of an abrupt-junction varactor tripler as a function of normalized load resistance x_3.

Fig. 18

$X_3 = \frac{R_{out}}{R_s}$ = normalized load resistance

$m_1 = \frac{|S_1|}{S_{max}}$ = normalized elastance coefficient

$P_{norm} = \frac{(V_B+\phi)^2}{R_s}$ = normalized power

V_B = Breakdown voltage

ϕ = Contact potential

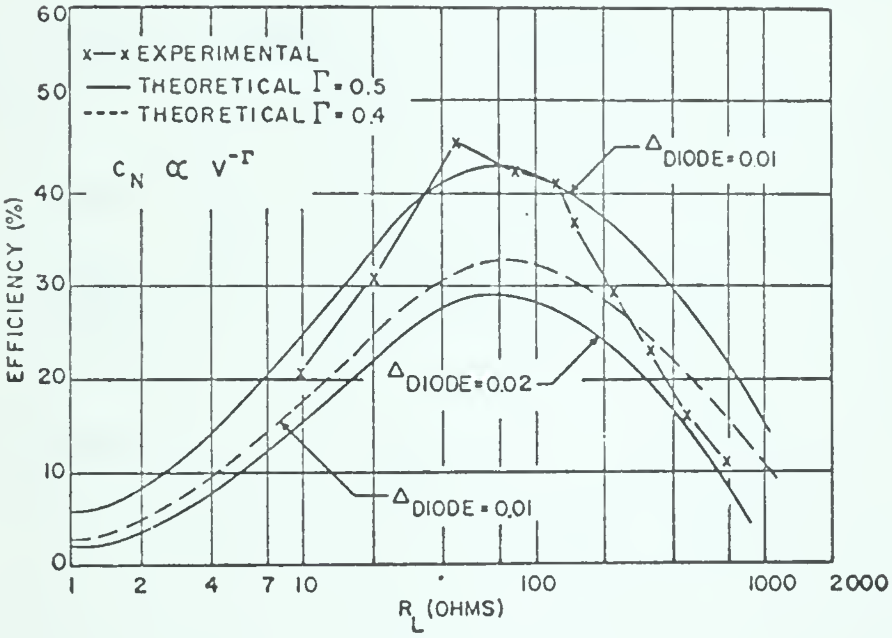


Fig. 19 Efficiency vs load resistance for 1-2-4-5 mode frequency quintupler.

Δ_{Diode} = normalized loss factor

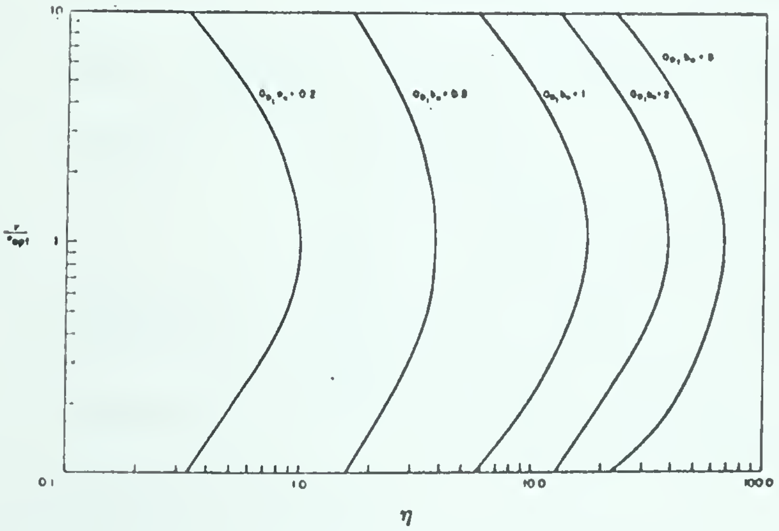


Fig. 20 -Efficiency vs normalized load to diode conductance coupling.

$V = \frac{n\omega_o}{G_{D_1}}$ = output diode Q

$\frac{n\,\omega_o}{G_{D_1}}$ = input diode Q

b_n = charge Fourier coefficient

to compare the results directly because of different input and output frequencies. The results of figure 19 are for an input frequency of 2.8Mc. and an output frequency of 14Mc.

Diamond's curves are far superior in that efficiency is plotted versus ω_{out}/ω_c where ω_c is the cutoff frequency of the varactor. This cutoff frequency is the figure of merit of varactors and on basis of this ω_c the performance of different diodes can be compared directly.

Results by K.M. Johnson ⑫ compare favorably with those of Diamond ④. Although their results are given in a somewhat different form they can be transformed so that results from both papers can be compared directly at least for the case of a frequence doubler. It is well to note that Johnson gives an analysis for a series connected varactor (voltage controlled) and Diamond's analysis is for a shunt connected varactor (current-controlled). Since Johnson doesn't use idler circuits in his analysis (whereas Diamond does) we can only compare their results for a doubler for which no idlers are required.

Results from Diamond's analysis are given in a slightly different form in a manual published by Varian Associates ⑯ (Beverly, Mass.). There we find for a doubler that,

$$\eta_{opt} = \frac{\sqrt{1+\left(\frac{m_1}{2}\frac{\omega_c}{\omega_0}\right)^2} - 1}{\sqrt{1+\left(\frac{m_1}{2}\frac{\omega_c}{\omega_0}\right)^2} + 1}$$

(Derived from Diamond's analysis)

Where,

$$\sqrt{1+\left(\frac{m_1}{2}\frac{\omega_c}{\omega_0}\right)^2} = \frac{R_{Lopt}}{R_S} = \frac{R_{in\,opt}}{R_S}$$

and m_1 is a function of the drive level ($m_1 = \frac{|S_1|}{S_{max}}$ where S_1 (elastance coefficient) $\propto I_1$, the input current); ω_c is the diode cutoff frequency; ω_0 is the input frequency; R_S is the diode series loss and R_1 is the load resistance. Johnson writes his multiplier effiency as:

$$\eta_{opt} = \frac{\sqrt{1+(Q_{D_1} b_n)^2} - 1}{\sqrt{1+(Q_{D_1} b_n)^2} + 1}$$

(see P. 529 ⑫ of Johnson's analysis)

where

$$\sqrt{1+(Q_{D_1} b_n)^2} = \frac{G_{Lopt}}{G_{Dn}}$$

where G_{Dn} is the equivalent diode loss conductance at the output frequency, and,

$$Q_{D_1} \equiv \frac{\omega_0 C_0}{G_{D_1}} \qquad b_n \equiv \frac{a_n}{C_0 V_1}$$

So,

$$Q_{D_1} b_n = \frac{\omega_0 a_n}{G_{D_1} V_1} = \frac{\omega_c}{\omega_0}\frac{i_n}{n V_1}$$

and for a doubler

$$Q_{D_1} b_2 = \frac{\omega_c}{\omega_0}\frac{i_2}{n V_1 C_{min}}$$

where i_2 is the magnitude of the output current, V_1 is the magnitude of the input voltage, and C_{min} is the minimum diode

capactiance.

If the results of the two analyses are to be the same then it is required that

$$\frac{m_1}{2} = \frac{i_2}{2V_1 C_{min}} \qquad \text{or} \qquad m_1 = \frac{i_2}{V_1 C_{min}}$$

Now for a doubler the input current magnitude is the same as the output current magnitude ⑬ and so the requirement is now $m_1 = i_1/V_1 C_{min}$.

From this we conclude that the analysis of both Johnson and Diamond give very similar if not completely identical results for the specific case of a doubler. It is difficult to check from either analysis whether the drive parameter, m_1, of Diamond is equivalent to the factor $i_1/V_1 C_{min}$ given by Johnson. This equivalence may not necessarily hold since Diamond assumes his varactor to be shunt connected whereas Johnson treats the dual series connected case.

If R_L/R_{Lopt} is plotted, both Diamond's results and those of Johnson give curves similar to figure 20 (from Johnson ⑫). We can further plot,

$$\eta = \frac{\sqrt{1 + \{K(I_1)\}^2} - 1}{\sqrt{1 + \{K(I_1)\}^2} + 1}$$

which is done in figure 21, where $K(I_1)$ is a function

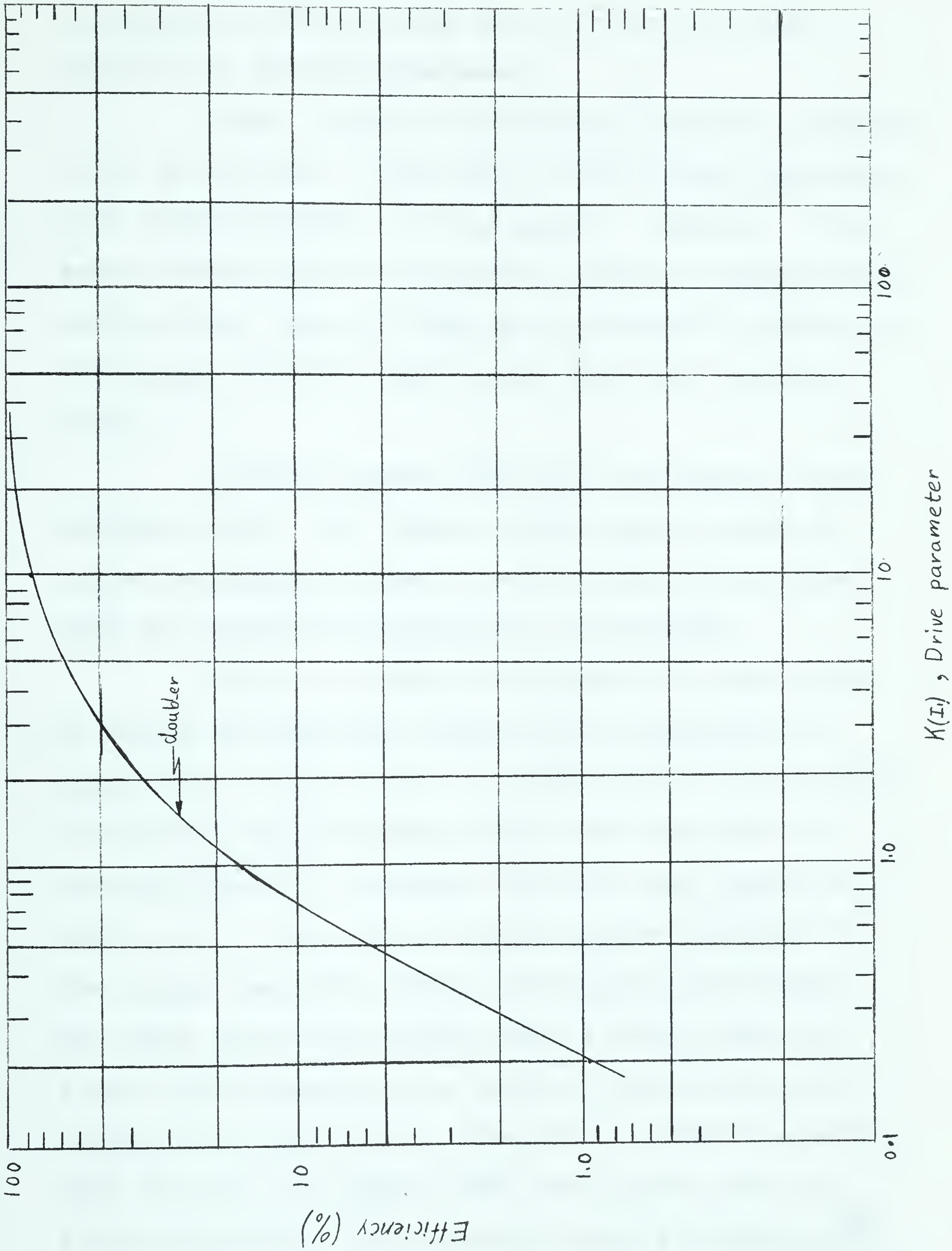


Fig. 21 Doubler Efficiency versus a Drive Parameter, $K(I_1)$

of the drive level as well as a function of diode quality and operating frequency.

Thus, a plot of efficiency versus the parameter $K(I_1)$ is obtained. Note that the efficiency approaches 100% asymptotically as $K(I_1)$ goes to infinity. This means, since there can only be a limited voltage swing on the diode, that ω_c must go to infinity to obtain an efficiency of 100%. This is the case for a lossless diode.

Johnson further plots the efficiency versus harmonic number (see figure 23) but such a graph is almost meaningless unless a set of curves is plotted with the normalized frequency as a parameter.

This can be done if the data for such a set of curves is taken from figure 8.60 in reference 2 (page 426). This results in figure 22 and gives a good indication how efficiency varies with the order of multiplication for varactors with the same figure of merit, ω_c. This set of curves applies strictly to the abrupt junction varactor multiplier even though for other varactors similar results can be expected. Figure 22 is based on data obtained from an analysis identical to that of B.L. Diamond ④. It must be noted here that all the higher order multipliers given in figure 22 contain idler circuits whereas Johnson's ⑫ figure 23 does not include idler circuits.

Reproduced in figure 24 is a graph, given in

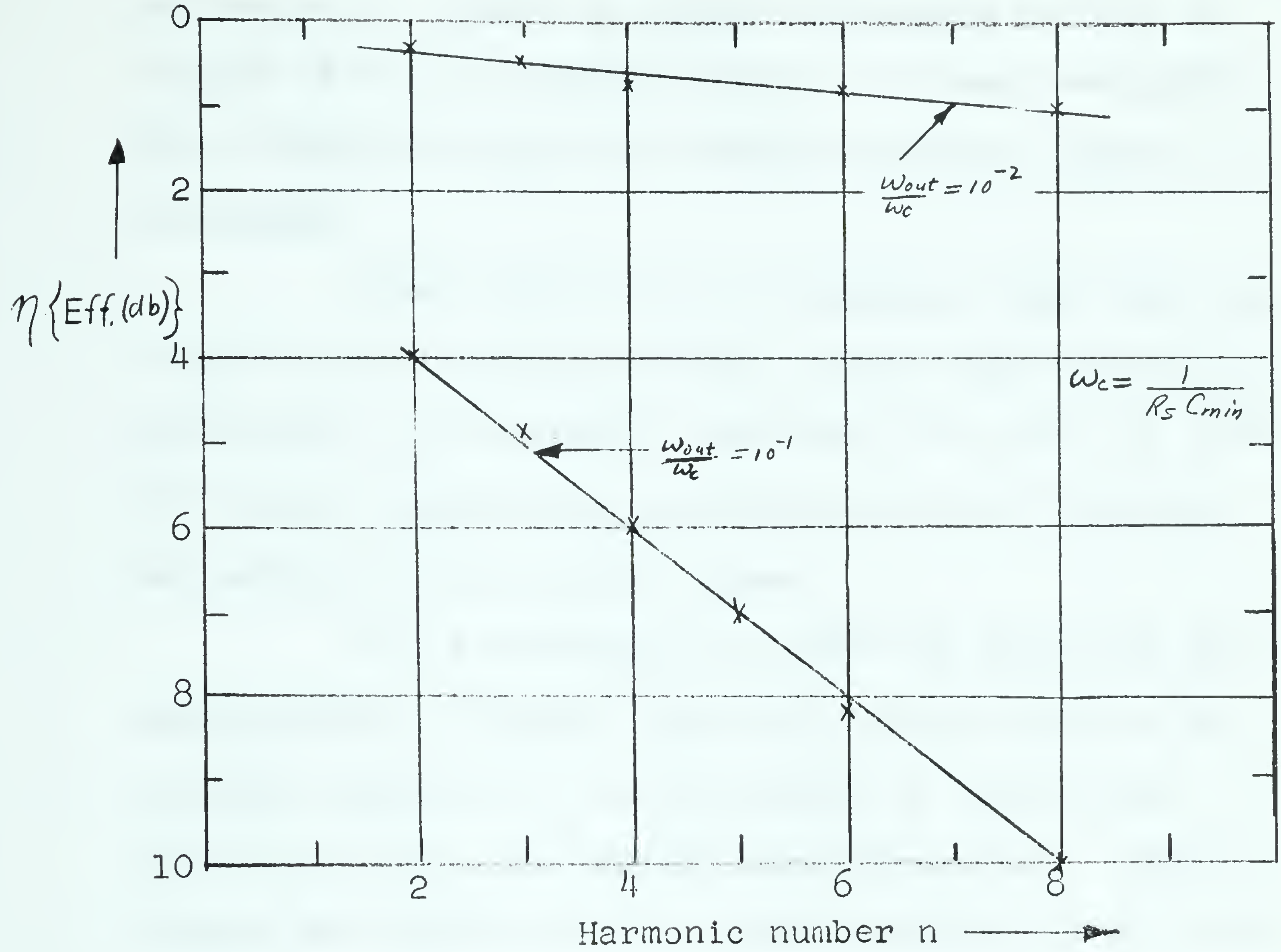
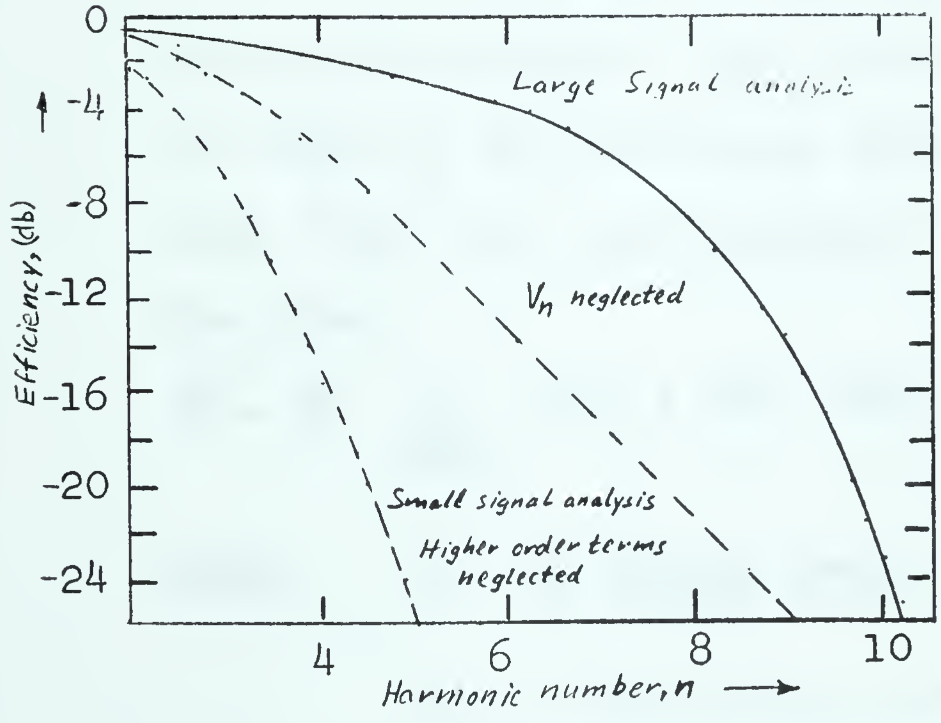


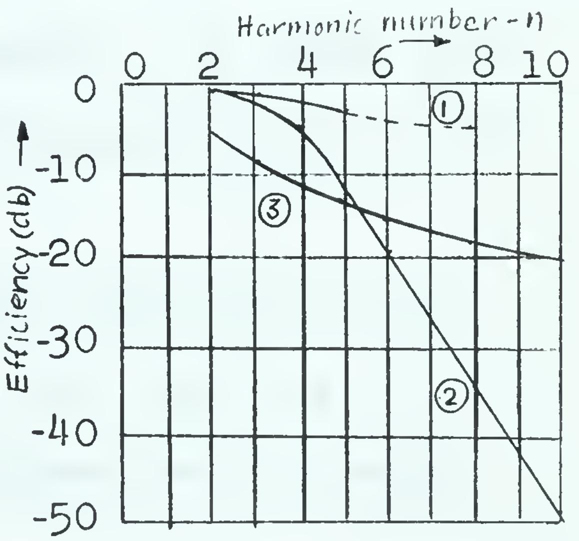
Fig. 22 Maximum Efficiency versus Harmonic Number for Abrupt Junction Varactors with Operating Frequency as a Parameter



For Hughes diode

$C_0 = 1\ \mu\mu f$; $R_s = 4$ ohms

Fig. 23 Conversion Loss versus Harmonic Number



① Nonlinear reactance (Utsonomyia, Yuan)
② Nonlinear reactance (Leeson and Weinreb)
③ Ideal resistive diode ($1/N^2$)

Fig. 24 Effiency versus Harmonic Number for Nonlinear Diodes

reference 11, which is similar in nature to that of figure 23 but, as already stated, is less meaningful than figure 22 since the results obviously depend on frequency.

From figure 22 it is apparent that even the higher order multipliers have a very high theoretical efficiency at frequencies for which $\omega_0/\omega_c < 10^{-2}$. Of course, experimental efficiencies would be less depending on the circuit losses.

It is worthwhile to note the fact that the efficiencies of higher order multipliers seem to be related linearly to the efficiency of lower order multipliers at a specified output frequency. Even though the curves are only approximately linear it is still a very useful approximation.

In a recent letter to the IEEE Proceedings ⑳ we see that Grayzel also has found linear relationships for some of the multiplier parameters. He shows that both input and output powers of the multiplier are of the form:

$$P_k = B_k \frac{\omega_o}{S_{max}} (V_{BD} + \phi)^2 \quad \text{with the restriction that} \quad \omega_o \ll \omega_c$$

where k = an integer which determines the output frequency ($k\,\omega_o$).

B_k = a constant at a specific frequency.

ω_o - the input frequency.

$\omega_c = S_{max}/R_s$ = the cutoff frequency.

S_{max} = the maximum value of diode elastance.

R_s = Series diode resistance.

V_{BD} = Varactor breakdown voltage.

ϕ = contact potential.

This, Grayzel says, implies that one can design an experimental model of a multiplier at some convenient low frequency and then scale this multiplier to any higher frequency since the input and output power are monatomically increasing functions of frequency.

From figure 22 it is apparent that efficiency also seems to be linearly related to frequency for $\omega_{out}/\omega_c < 10^{-2}$. This result is not obvious from Grayzel's work but it seems plausible that his remarks could be extended to give a relationship relating the efficiencies of high-and low-order multipliers.

In any case, even though the curves of figure 22 are only approximately linear they are indeed useful in extrapolating to higher order multipliers with the same ω_{out}/ω_c ratio and thus arriving at a fair indication of the efficiency of such a multiplier. Even for normalized frequencies of the order of $\omega_{out}/\omega_c = 10^{-1}$ this method could be used as a first approximation to the multiplier efficiency of a high-order multiplier.

It is also noted that Grayzel's results can be deduced directly from the low-frequency asymptotes of the multiplier characteristics given by Diamond ⑪ and Rafuse and Penfield ②.

2.3.2 - Graded Junction Varactor Multiplier

Both the theoretical and experimental varactor multiplier characteristics for this case are very similar to those of the abrupt junction device. Greenspan (see appendix F of ②) has calculated some theoretical results for a graded junction varactor doubler. These results come from an analysis very similar to, but more complex than that of Diamond ④,②. And as could be expected the efficiency and other characteristics are qualitatively the same as those obtained by Diamond, except that the efficiency for the graded junction device is slightly lower. The actual curve, very similar to that of the doubler in figure 15, is not given here.

Furthermore we find evidence in the literature ㉑ that the efficiency of a varactor multiplier is a function of Γ, where $C(v) = C_o/(V + \phi)^{\Gamma}$. This paper indicates that the efficiency becomes a maximum for $\Gamma \doteq 0.6$.

There is little further evidence in the literature of how the graded junction behaves in a multiplier. Generally speaking, the theory and results of an abrupt junction varactor can be used as an initial design for graded junction devices which can then be optimized experimentally.

2.3.3 - Special Diffused Junction Varactor Multiplier

This type of varactor is of fairly recent origin and has considerably advanced the borders of the "State

of the Art" in solid state multipliers. A recent article by G. Schaffner ⑤ discusses the qualitative aspects of this varactor and indicates performance limits. No theoretical results are given for multiplier operation. However, different circuits are presented which, using the special varactor, yield high conversion efficiencies and allow high power handling. For further comments on the actual circuits see section 2.4.3.

2.3.4 - Surface Varactors and p-n Junction Varactors under Forward Bias

None of the varactors which exhibit an exponential capacitance-voltage dependence have been analyzed until now. However, a few qualitative statements can be made about an actual multiplier taking advantage of an exponential characteristic displayed when the varactor is driven into the forward voltage region.

Leeson ① in his paper refers to a quintupler, with no idler current paths, which yielded an efficiency for multiplication in excess of 40% (340Mc - 1700Mc). The varactor was driven into the forward bias region and good efficiency and high power output was obtained. Leeson gives values of efficiency and power output for this quintupler using three different diodes. The capacitance and shunt series resistance of each diode was also measured for a forward bias up to + 0.48 volts. The highest efficiency resulted for the diode whose capacitance increase was largest for a small forward bias increase. From this it is assumed that the exponentially dependent

diffusion capacitance of the varactor diode was mainly responsible for the increase in efficiency, all other characteristics being the same for all three diodes.

2.4 - Circuit Configurations for the Different Types of Multipliers

Here we will give typical proven circuits and compare their simplicity, effectiveness, output purity, and efficiency. In our discussion on varactor circuits it is well to remember that first of all the circuit must allow only currents or voltages of certain specified frequencies to exist. Secondly, in most practical circuits the reactance of the varactor at the different frequencies must be tuned out. Finally, the varactor input and output impedance must be properly matched to the generator and the load to insure maximum power transfer and a minimum disturbance to the system especially at higher frequencies.

2.4.1 - Circuits with the Varactor current-driven

One group of researchers (13) has come up with a few very practical circuits which give good results at frequencies in the 100-500 Mc range. One of these is a lumped circuit for a high efficiency frequency doubler as shown in figure 25.

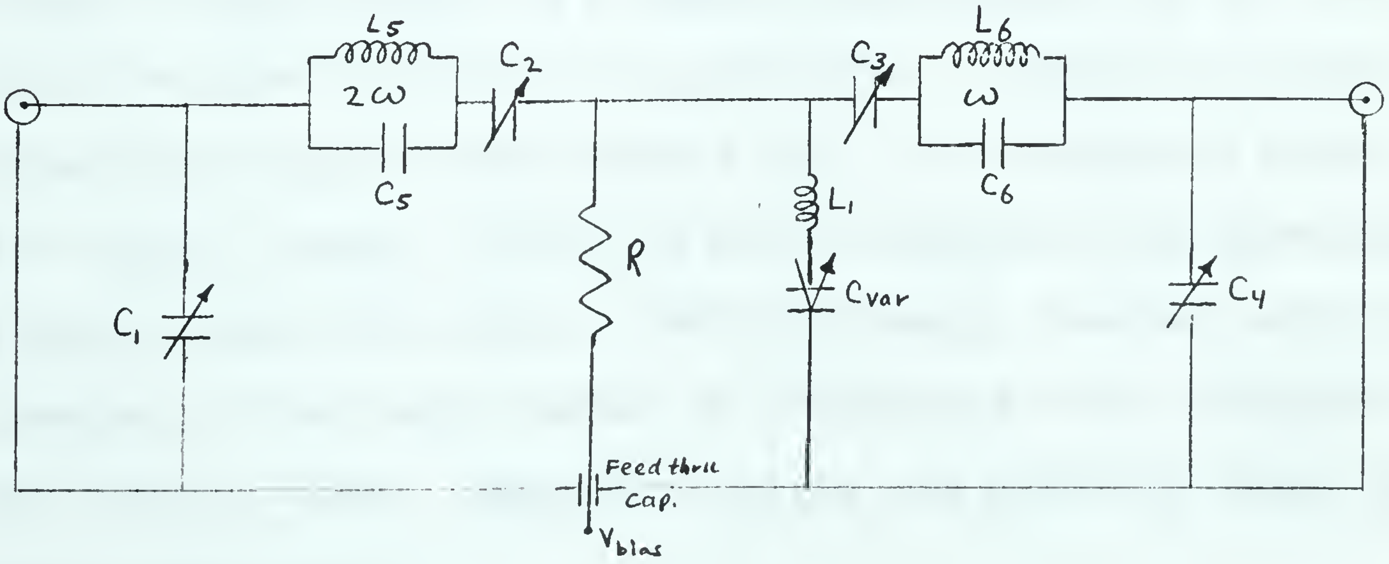


Fig. 25 Frequency Doubler Circuit

L_1 is designed to have one-half the calculated value of inductance needed to resonate with C_{var} at the input frequency. This value then determines the trap capacitances C_5 and C_6. C_1, C_2, C_3, and C_4 are used for trimming and matching.

Reducing the number of components decreases the overall circuit loss and thus increases the multiplier efficiency. However, the filtering of higher harmonics at the output may also be weakened in which case either external filters must be used or traps resonant at the higher frequencies can be incorporated in the actual circuit itself. A detailed example of this more complex type of circuit is given by B.L. Diamond ④ in his thesis (see figure 26 for a reproduction of his circuit).

A complete synthesis of a quadrupler is given by Diamond. He has not included any impedance transformations in order to make his synthesis independent of the varactor used. Note, however, that allowing impedance transformations, which is often necessary for matching input and output, would result in a simplified network but in turn would be more difficult to synthesize. Diamond's circuit should give good output purity (w. r.t. frequency) since the first, second, fifth and sixth harmonics are essentially blocked from the output. The efficiency, however, will suffer because of the large number of components which increase the circuit loss. Component values are given in terms of C_o in reference 4.

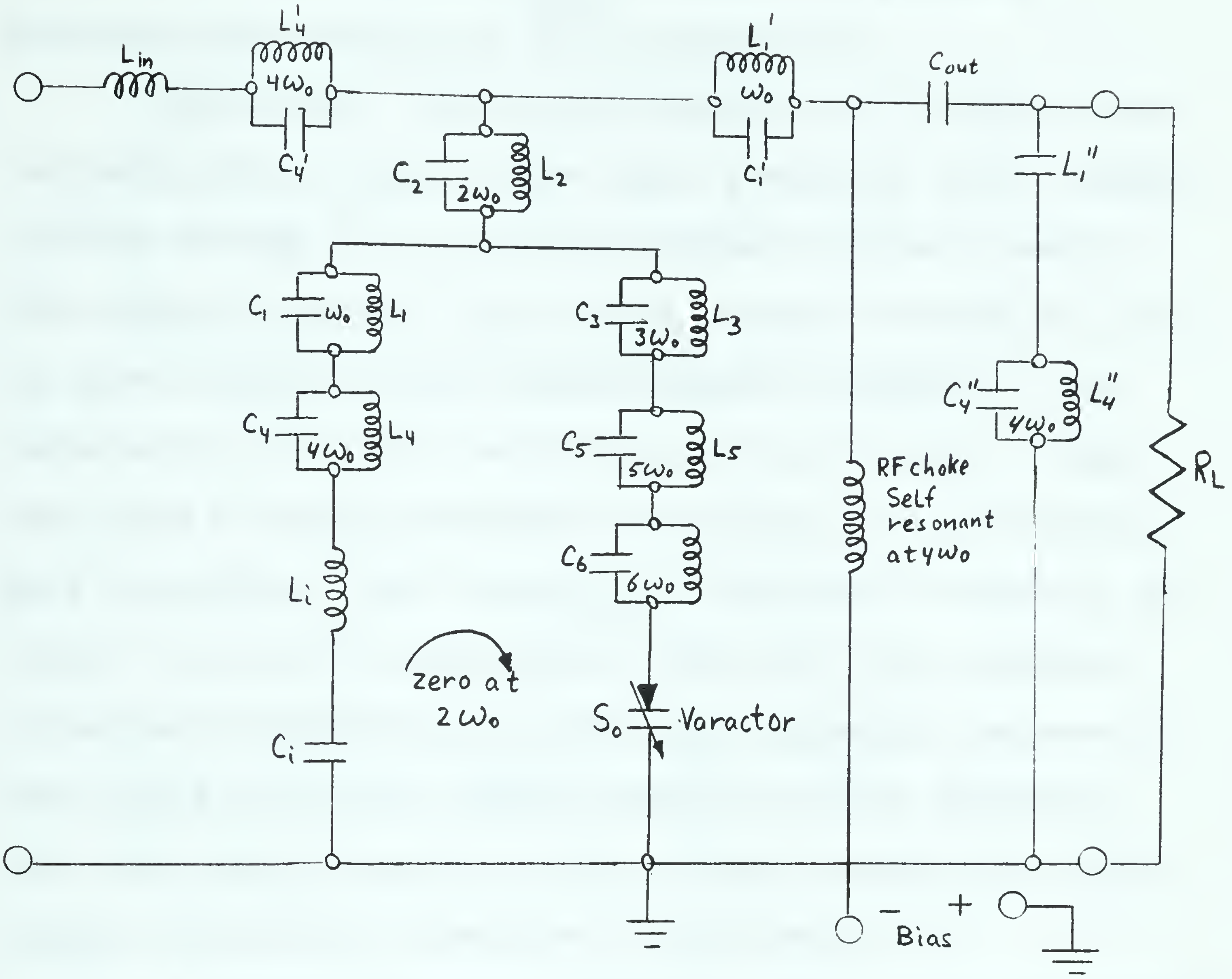


Fig. 26 Circuit Diagram for an Abrupt Junction Quadrupler

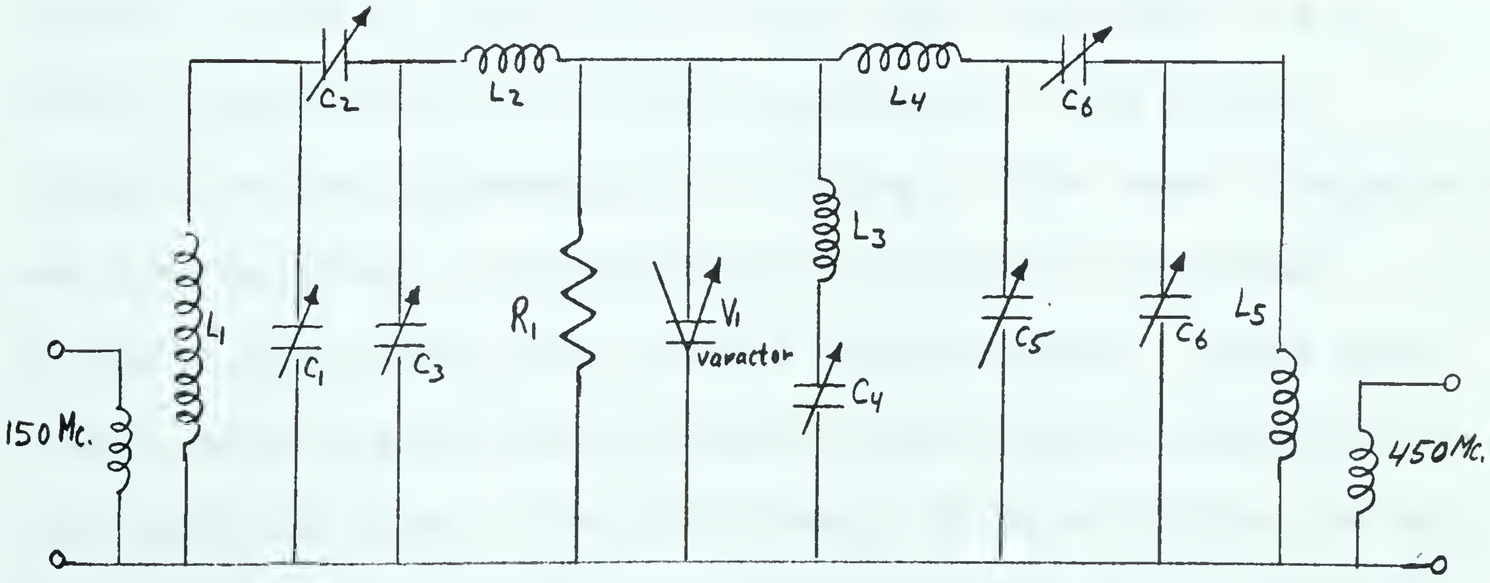


Fig. 27 Frequency Tripler Circuit (150-450 Mc.)

Another very effective circuit is given by Microwave Associates Inc. ㉒ in figure 27.

Basically, the circuit consists of a double tuned bandpass filter tuned to the input frequency (L_1C_1, $L_2C_3V_1$ coupled through C_2), a similar bandpass filter tuned to the output frequency (L_5C_7,$L_4C_5V_1$ coupled through C6), and an idler circuit at the second harmonic ($L_3C_4V_1$). The resistor R_1 provides a self bias to the varactor. They also give a tuning procedure for tuning a circuit with so many variables. This circuit will deliver 10 watts at the output at an efficiency greater than 50% (for component values see reference 22). Spurious frequency response is also found to be well below (-30db) the output frequency for this fairly simple circuit. Other lumped and coaxial cavity circuits are described in reference 16.

A simple frequency doubler, useful from 500-5000Mc/s, made from coaxial slab line is shown in figure 28. The lengths l_1 and l_2 are found by taking into account the diode capacitance, usually the average capacitance C_o, and making l_1 and C_o resonant at the input frequency and l_2 and C_o resonant at the output frequency. The center conductors are adjustable for tuning to the exact frequencies and the varactor is mounted in the region of maximum electric field with its cathode end grounded. Input and output matching can be achieved by varying the position of the coupling disks. The efficiency of this doubler is very good but its poor output spurious response often requires

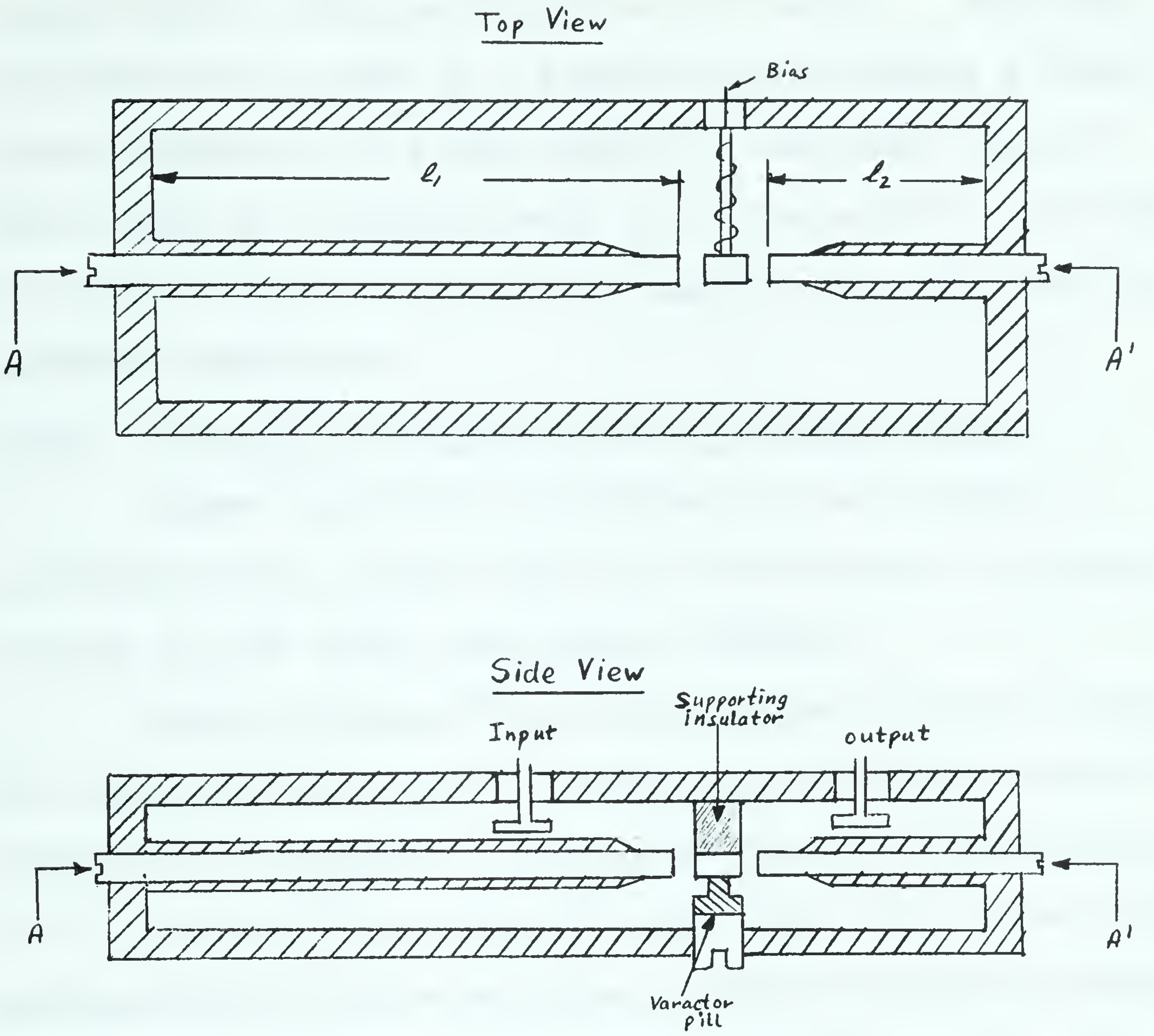


Fig. 28 Simple Microwave Varactor Doubler (useful for 500 Mc/s to 5KMc/s)

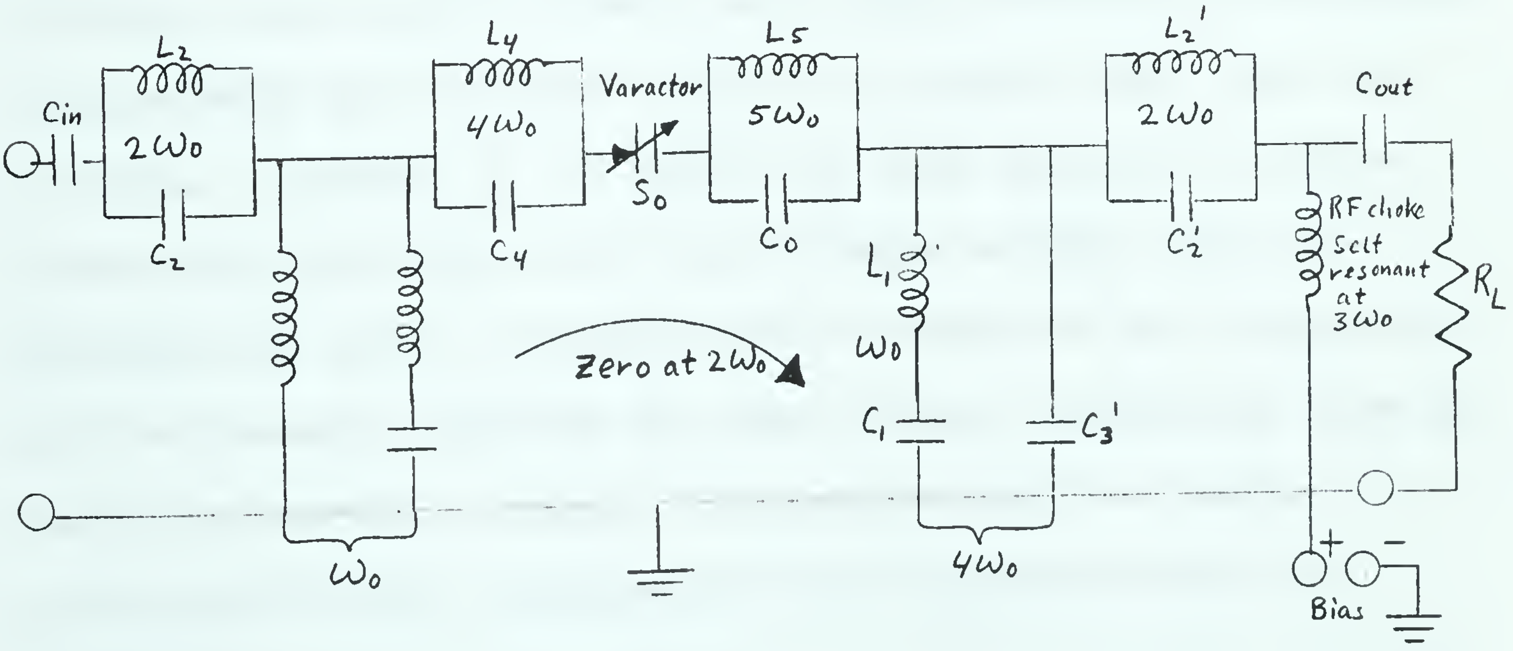


Fig. 29 Circuit Diagram for an Abrupt Junction Tripler

an additional bandpass filter at the output. Efficient triplers can be made in a similar way by adding a third center conductor at right angles to the other two and also coupling it capacitively to the varactor so that now an idler circuit is present to improve the efficiency of harmonic generation.

2.4.2 - Circuits with the Varactor Voltage Driven

These circuits are similar to the current-controlled ones, except that now the varactor is series coupled to the input and output circuits.

Again, Diamond ④ has synthesized a tripler, using the configuration shown in figure 29, and gives values for components in terms of the average varactor capacitance.

Rafuse ② and others ④ state that the current driven configuration is more efficient than the voltage controlled multiplier. However, there seems to be little indication, with the circuits presently used, to prefer one above the other except for the fact that the current controlled varactor can usually handle more power because its cathode is grounded and is hence easier to provide with good heat sinking. Further it is useful to note that for voltage controlled varactors all the voltages except the ones desired are short circuited but currents at all frequencies can be present; whereas for the current controlled case all varactor currents except the ones desired are open-circuited but now voltages at all frequencies may be present.

2.4.3 - High Power Circuits

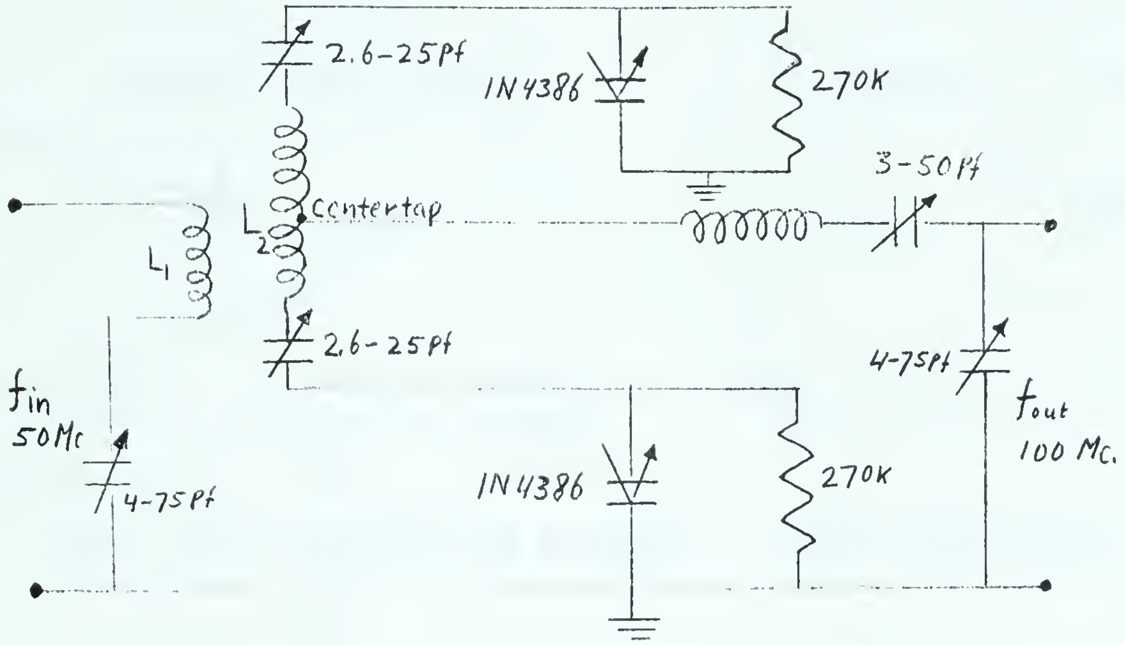
Using bridge, push-pull, and push-push circuits the power output of multipliers can be increased considerably. Rafuse ② indicates a symmetric bridge circuit for a frequency doubler (page 337 ②). Even and odd harmonics are automatically separated by this bridge construction which thus requires fewer harmonic "traps" and, of course, since four varactors are used it also increases the power capability four times.

A push-push circuit (see figure 30) is given by G. Schaffner which has a power output of 180 watts at 100 Mc, with a 70% efficiency. It must be noted that the high power output here is not only a result of the circuit configuration. Schaffner has used a new type of diode which basically can handle more power because of improved construction and varactor characteristics. He also reports a tripler, 50-150 Mc, with 70% efficiency for a power input of over 50 watts, and another tripler, 150-450Mc, with over 50% efficiency for a power input of 40 watts.

2.4.4 - Odd Harmonic Circuits

By using two voltage controlled, parallel varactors biased in opposition, it has been shown by W.R. Avellino ㉓, by means of a small signal approximation, that only odd harmonics of the fundamental driving frequency are present in the current waveform produced by an even C-V characteristic.

A circuit to obtain such a characteristic is given in figure 31 and the composite C-V characteristic is shown



L_1 = 3 turns #10 wire, 1" Dia.

L_2 = 10 turns #10 wire, 1" Dia.

L_3 = 1 turn #10 wire, 3/4" Dia.

Fig. 30 High Power Push-Push Doubler (50-100 Mc)

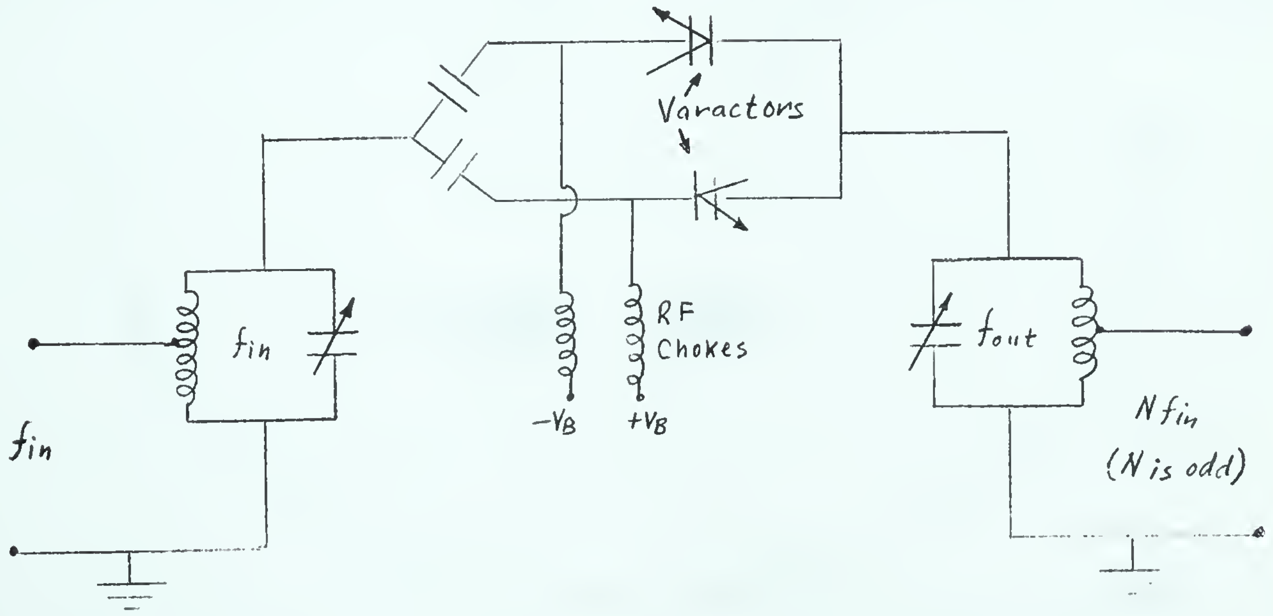


Fig. 31 Series-Connected Opposingly Biased Varactor Multiplier for Odd Harmonic Generation

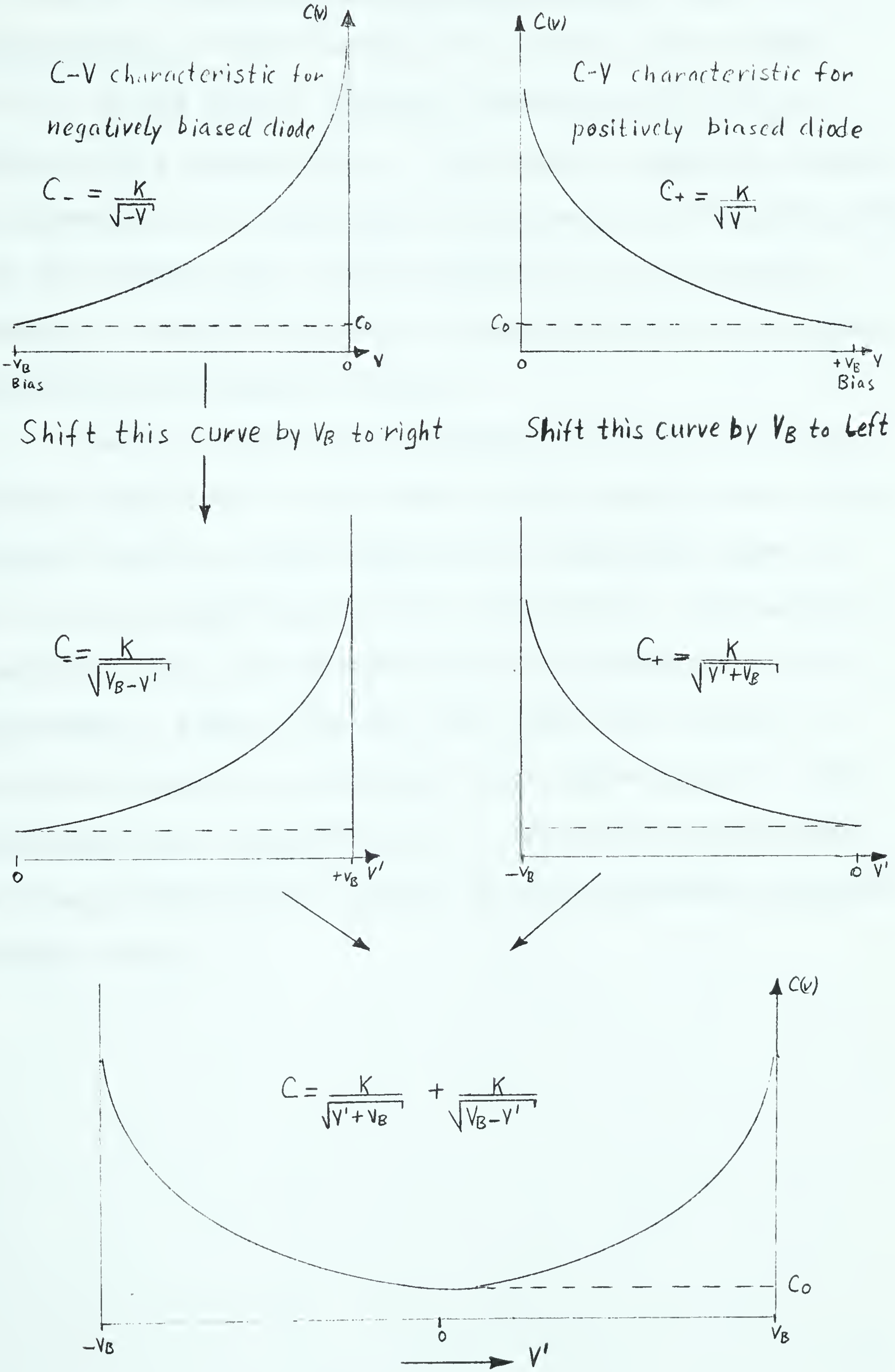

C(V)
C-V characteristic for negatively biased diode
$C_- = \frac{K}{\sqrt{-V}}$
C₀
$-V_B$ Bias
0
V
C(V)
C-V characteristic for positively biased diode
$C_+ = \frac{K}{\sqrt{V}}$
C₀
0
$+V_B$ Bias
V
Shift this curve by V_B to right
Shift this curve by V_B to Left
$C = \frac{K}{\sqrt{V_B - V'}}$
0
$+V_B$
V'
$C_+ = \frac{K}{\sqrt{V' + V_B}}$
$-V_B$
0
V'
C(V)
$C = \frac{K}{\sqrt{V' + V_B}} + \frac{K}{\sqrt{V_B - V'}}$
C₀
$-V_B$
0
V_B
V'

Fig. 32 Composite C-V Characteristic for Series-Connected Opposingly Biased Varactors.

in figure 32 for two parallel diodes oppositely biased. This paper ㉓ also gives some experimental data on a doubler and a tripler using the opposing bias scheme as well as the direct parallel connection of the two diodes with a common bias. The results indicate clearly an improvement in conversion efficiency for tripling using this new scheme with large suppression of the second harmonic. The 2^{nd} harmonic is approximately 20 db down from the third harmonic output.

Hence, from the discussion in section 2.1.4 on surface varactors we can deduce quite easily that for a surface varactor which exhibits an inversion layer as well as an accumulation layer capacitance, odd harmonic generation will be enhanced and even harmonics will be suppressed. Apart from the fact that this scheme of varactor connection generates only odd harmonics, thus reducing filter requirements, it also has larger power handling capability by nature of the increased effective voltage range.

CHAPTER 3

LARGE SIGNAL ANALYSIS OF AN N-TIMES MULTIPLIER USING AN ADMITTANCE MATRIX APPROACH

3.1 Introduction

In this chapter a large signal analysis of an N-times frequency multiplier is given with the varactor series connected in the circuit. This analysis is quite general and can basically be applied to any capacitance-voltage characteristic. Some of the arguments concerning the diode loss conductance, G_D, in section 3-2 apply specifically to a varactor driven into the forward voltage region since the analysis of the forward voltage region is a primary reason for the development of this general multiplier theory. Many practical multipliers with self-biased varactors also drive the diode into the positive voltage region to obtain increased power output and efficiency. Thus there is good reason for the arguments given.

Section 3.4. is completely general and gives the operating parameters of the multiplier in terms of the Fourier capacitance coefficients. In a later chapter this theory is applied to a specific varactor frequency multiplier.

Basically, the approach is concerned with finding the admittance parameters of the varactor treated as a two part network. Once these parameters are determined the conversion properties of the varactor can then be completely specified. One can obtain the operating parameters of the multiplier in terms of the capacitance Fourier coefficients which in turn are obtained from a Fourier series expansion of the highly nonlinear capacitance function.

3.2 - Equivalent Diode Circuit

In this analysis only voltage controlled multipliers will be considered. The reason for this choice can be made clear by considering the forward voltage region of an arbitrary diffused junction varactor diode. This region can be regarded as representing a low-loss nonlinear capacitor as indicated by Leeson ①. Referring to figure 33(a) observe that driving the diode into the forward voltage region results in a large increase in charge for a relatively small voltage increase. Coupling between the input and output tuned circuits of the multiplier in this case is a maximum at maximum capacitance (see figures 33b, 33c). It is thus quite logical that the resulting charge wave-form will exhibit a marked increase in harmonic content. (note: The multiplier circuits, shown in figure 33c and 34c, are greatly simplified to make the distinction between charge control and voltage control clear).

For figure 34, the current or charge-controlled case, the diffusion effect (dotted lines) only changes the way in which the elastance approaches zero (figure 34b) and flattens the V-Q curve (figure 34a) somewhat. However, since this occurs at a point of minimum coupling (minimum elastance), we would not expect the multiplier operating parameters to change appreciably. This effect would particularly manifest itself in the higher order multipliers since without this extra nonlinearity the harmonic content is mainly second harmonic.

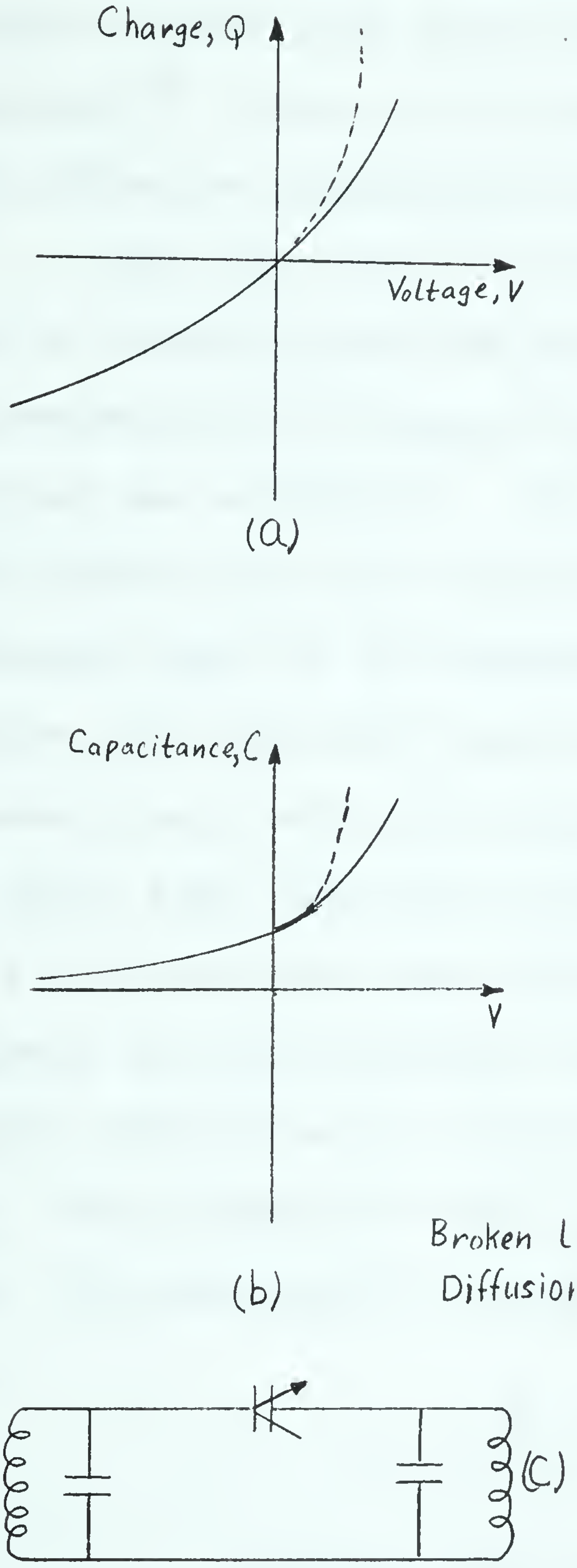


Fig. 33 Q-V and C-V Curves for Voltage-Controlled Varactor

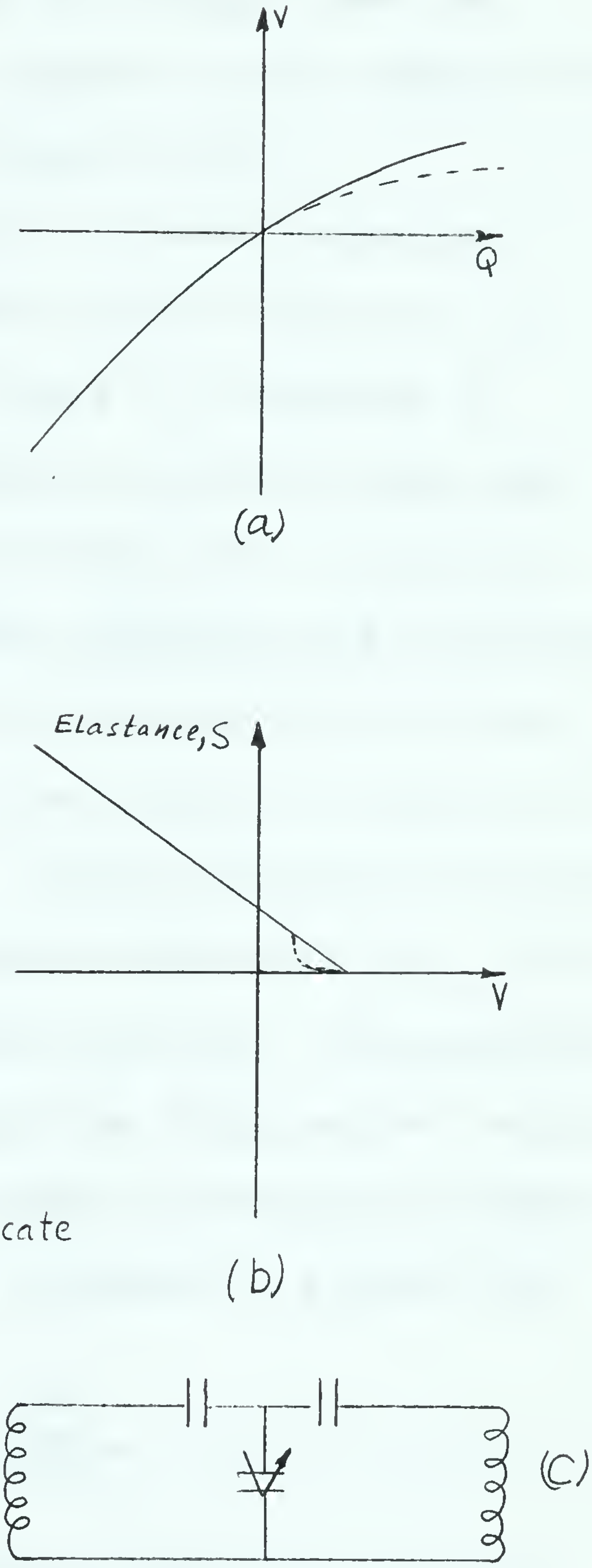


Fig. 34 V-Q and S-V Curves for Current-Controlled Varactor

Broken lines indicate Diffusion effect

This higher harmonic content of the voltage controlled "overdriven" case should lead to reasonably high conversion efficiencies for high orders of multiplication with or without the use of idler circuits. We would still expect idlers to enhance the efficiency (this allows mixing effects) but

they would not be as essential to efficiently generate the higher harmonics as in the case of the abrupt junction varactor ④. (Note: For further remarks on the behavior of the diffusion capacitance see section 2.1.4).

From the previous discussion it seems reasonable for us to use a parallel equivalent circuit since we are concerned with voltage and capacitance (as opposed to current and elastance). It is widely accepted today that the series equivalent circuit (see figure 35) is quite an accurate model of the varactor under reverse bias conditions. In the case when the varactor is driven positive, however, a shunt loss conductance appears even though in practice it is small (see reference 1 and 7). In any case we will have to find some value for a shunt diode conductance, G_D, since we want to use a parallel equivalent circuit. An equivalent shunt conductance can be found from the diode series resistance, R_s. This conductance will, of course, be frequency dependent. The equivalent circuit used is given in figure 36b.

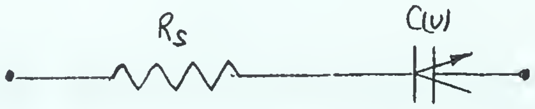


Fig. 35 Varactor Series Equivalent Circuit

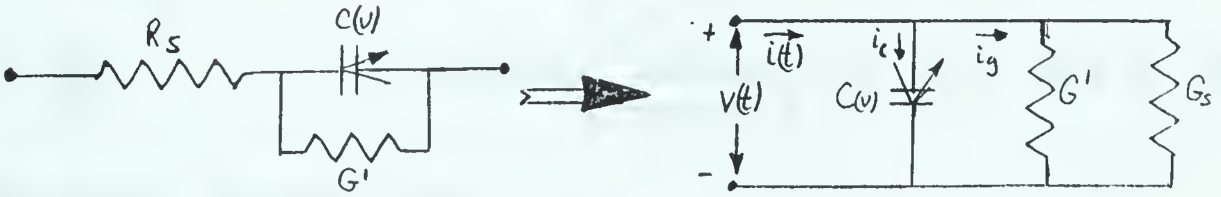


Fig. 36 a

Fig. 36b
Varactor Parallel Equivalent Circuit

The admittance of the circuit in figure 36a is given by

$$Y = \frac{1}{R_s + \frac{1}{G' + j\omega C}} = \frac{G' + j\omega C}{R_s G' + j\omega C R_s + 1} = G + jB$$

Multiplying the numerator and denominator by the complex conjugate of the denominator and separating real and imaginary parts yields,

$$G = \frac{G' + R_s G'^2 + \omega^2 C^2 R_s}{(R_s G' + 1)^2 + \omega^2 C^2 R_s^2}$$

$$B = \frac{\omega C}{(R_s G' + 1)^2 + \omega^2 C^2 R_s^2}$$

For practical good quality diodes $R_s \ll \frac{1}{\omega C}$ and $R_s G' < 1$ (see also page 54) and using this in expressions for G and B gives,

$$G = G' + \omega^2 C^2 R_s$$

$$B = \omega C$$

Then by comparison with figure 36b we see that $G_s = \omega^2 C^2 R_s$. (1)

The conductance G_s in figure 36b is thus the parallel equivalent of R_s, and G' is the shunt conductance appearing under forward bias. According to Leeson ^{1}, the shunt diode loss, G', for a positively biased varactor is small and constant over a wide frequency range and for long lifetime diodes.

Next it is desired to obtain an expression for the total diode quality factor Q_D.

Let, $Q_R = \frac{1}{\omega C R_s}$ - Quality factor for figure 35 (R_s and C(v) only)

and $Q_G = \frac{\omega C}{G'}$ - Quality factor for C(v) and G' shunted across it.

Then the total diode Q is,

$$Q_D = \frac{1}{\frac{1}{Q_D} + \frac{1}{Q_G}} = Q_D = \frac{1}{\omega C R_s + \frac{G'}{\omega C}}$$

Now a cutoff frequency, ω_c, is defined as that frequency at which the diode Q becomes equal to unity.

Therefore,

$$1 = \frac{1}{R_s \omega_c C + \frac{G^1}{\omega_c C}}$$

and thus solving for ω_c yields:

$$\omega_c = \frac{1}{2R_s C_{min}} + \frac{1}{2R_s C_{min}} \sqrt{1-4\,G^1 R_s} \qquad (2)$$

Where C_{min} (the minimum diode capacitance) is used so as to give the highest possible ω_c.

For most low-loss diodes G^1 is of the order of one millimho① and R_s is of the order of one ohm, thus $4G^1R_s \ll 1$. Making this simplification,

$$\omega_c = \frac{1}{R_s C_{min}}$$

which is the usual definition of the diode quality factor when only series loss exists.

Substituting for R_s in terms of G_s by equation (1) thus results in,

$$\omega_c = \frac{\omega^2 C_{min}}{G_s} \qquad (3)$$

Where ω is the operating frequency, C_{min} is the minimum capacitance over the diode operating region, and G_s is the parallel equivalent of the series diode resistance R_s.

3.3 - Varactor Equations of Motion

From figure 36b we see that the instantaneous varactor currents are:

$$i_c(t) = \frac{dq}{dt} = \frac{dq}{dv}\frac{dv}{dt} = C(v)\frac{dv}{dt} = C(v)v(t)$$

Thus,

$$i_c(t) = C(v)\,\frac{dv}{dt} \qquad (4)$$

and

$$i_g(t) = G_D\,v(t) \qquad (5)$$

Where C(v) is the incremental diode capacitance, G_D is the total diode loss conductance, and v(t) is the applied voltage. Adding equations (4) and (5), the total varactor current is obtained,

$$i(t) = G_D\,v(t) + C(v)\,\frac{dv}{dt} \qquad (6)$$

Let us now expand i(t), C(t), and v(t) into complex Fourier series so that,

$$i(t) = \sum_{k \neq o} I_k e^{jk\omega_o t} \quad \text{(exclude d.c. currents, i.e., } k \neq o\text{)} \qquad (7)$$

$$v(t) = \sum_{r} V_r e^{jr\omega_o t} \qquad (8)$$

$$C(t) = \sum_{m} C_m e^{jm\omega_o t} \qquad (9)$$

Substituting equations (7), (8), and (9) into (6) gives,

$$\sum_{k \neq o} I_k e^{jk\omega_o t} = \sum_{r} G_D V_r e^{jr\omega_o t} + \sum_{m} C_m e^{jm\omega_o t} \sum_{r} (jr\omega_o) V_r e^{jr\omega_o t}$$

or,

$$\sum_{k \neq 0} I_k e^{jk\omega_o t} = \sum_{r} G_D V_r e^{jr\omega_o t} + \sum_{m}\sum_{r} (jr\omega_o) C_m V_r e^{j(m+r)\omega_o t} \qquad (10)$$

Now multiply equation (10) by $e^{-jk\omega_o t}\,dt$ and integrate, hence,

$$I_k = \frac{1}{T}\int_0^T \sum_{r} V_r e^{j(r-k)\omega_o t}\,dt + \frac{1}{T}\int_0^T \sum_{r}\sum_{m} (jr\omega_o) C_m V_r e^{j(r+m-k)\omega_o t}\,dt \qquad (k \neq o) \quad (11)$$

Observe, that all the integrals on the R.H.S. of (11) are zero, unless,

$r = k$ for 1st integral

$r - m = k$ for 2nd integral

Using these conditions in equation (11) results in,

$$I_k = G_D V_k + \sum_{r} (jr\omega_0) C_{k-r} V_r \quad (k \neq 0)$$

or rewriting,

$$I_k = (G_D + jk\omega_0 C_0) V_k + \sum_{r \neq k} (jr\omega_0) C_{k-r} V_r \quad (k \neq 0) \qquad (12)$$

Equations (12) are sometimes called the "Varactor Equations of motion". Reference 2 describes the dual form of (12).

Note, that if only those frequency components allowed by the external circuit, in which the varactor is imbedded, are considered, then equations (12) are simplified immediately. Seeing that the varactor will be voltage pumped, only the voltages at the fundamental, idler (if any), and output frequencies are allowed to exist across the varactor. All other voltage components will be assumed shorted to ground by appropriate filters.

However, other current, and thus other capacitance Fourier components, may exist in the circuit eventhough these are not measurable from either input, output, or idler ports of the multiplier network (see also section 3.4). Currents at frequencies other than those allowed by the circuit are short circuit currents. These clearly would not contribute any power since no voltages can exist at these other frequencies. Nevertheless, as we shall see later, these other capacitance, or current components do determine the conversion properties of the multiplier.

3.4 - An N^{th} Harmonic Multiplier Without Idlers

3.4.1 - General Two-port Representation

Consider now the case where the input frequency, ω_0,

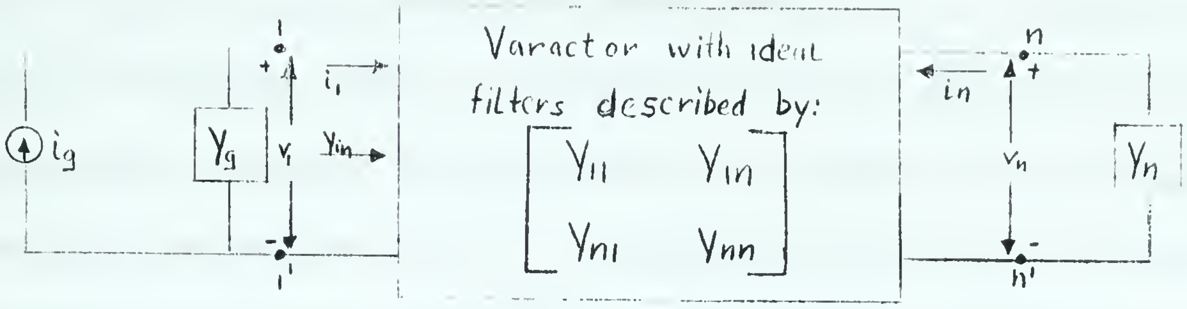


Fig. 37 Two-Port Multiplier Network

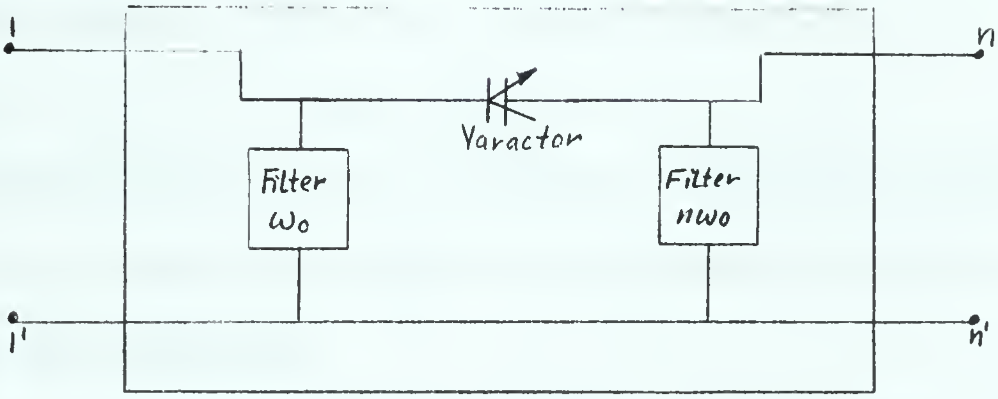


Fig. 38 Detailed Circuit of Varactor with Filters

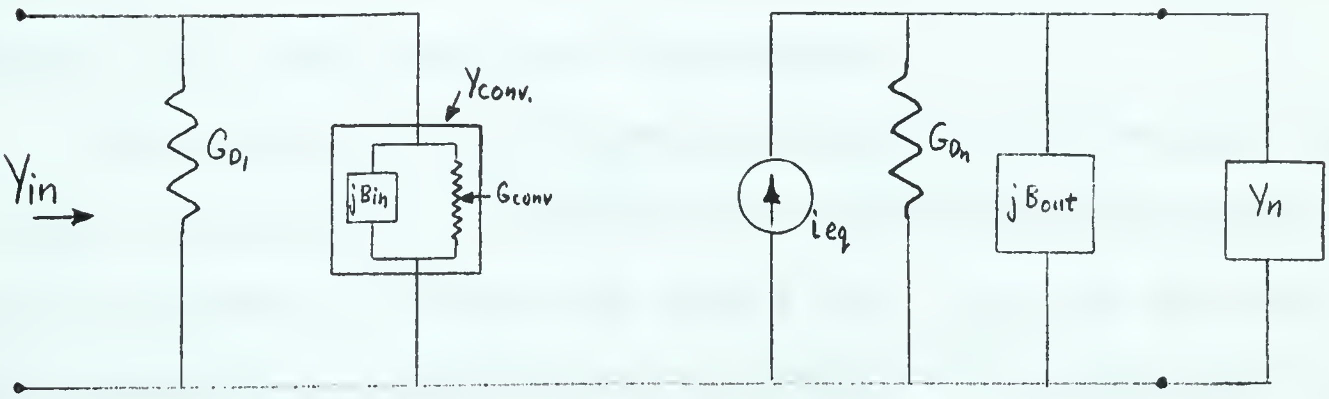


Fig. 39 Equivalent Multiplier Circuit

is multiplied to the output frequency, $n\omega_o$, using a varactor. We will consider such a varactor with appropriate filters, as a two-port network illustrated in figure 37 and figure 38. If we can determine the Y- parameters of this two-port, we can then completely describe the varactor behavior in a circuit.

The equations describing the two-port network of figure 37 are:

$$i_1 = Y_{11}v_1 + Y_{1n}v_n \qquad (13a)$$

$$i_n = Y_{n1}v_1 + Y_{nn}v_n \qquad (13b)$$

At the output there is a load constraint,

$$i_n = -Y_n v_n$$

Substituting this into equation (13b) and further substituting for v_n in equation (13a) an expression for the input admittance is obtained,

$$Y_{in} = \frac{i_1}{v_1} = Y_{11} - \frac{Y_{1n}Y_{n1}}{Y_{nn} + Y_n} = G_{in} + jB_{in} \qquad (14)$$

Similarly the output admittance is obtained from equations (13) hence,

$$Y_{out} = \frac{i_n}{v_n} = Y_{nn} - \frac{Y_{1n}Y_{n1}}{Y_{11} + Y_1} \qquad (15)$$

where $Y_1 = Y_g$, the generator admittance.

The multiplier efficiency can now be determined from the input conductance. Consider the equivalent multiplier circuit as shown in figure 39, where G_{D1}, G_{Dn} are the equivalent diode loss conductances existing at the input and output frequencies respectively, Y_n is the load admittance, Y_{conv} is the varactor conversion admittance (the useful part

of the input admittance) which is responsible for the power transfer from the input to the output frequence, B_{in} and B_{out} are simply the reactive components of the input and output admittances, and i_{eq} is an equivalent current source giving power output at the nth harmonic frequency. This i_{eq} is proportional to the conversion admittance of the input circuit. Part of the input and output power is clearly dissipated in the loss conductance G_D. Then from figure 39 we see that the ratio of input power dissipated in G_{conv} (this power is converted to the output frequency) to the total input power is,

$$\frac{\text{useful } P_{in} \text{ converted to } f_{out}}{\text{total } P_{in}} = \frac{\text{Re}\{Y_{conv}\}}{\text{Re}\{Y_{in}\}} = \frac{\text{Re}\{Y_{in}\} - G_{D1}}{\text{Re}\{Y_{in}\}} = \text{input circuit efficiency}$$

Similarly in the output circuit the ratio of useful output power reaching the load conductance to the total power present at the nth harmonic is,

$$\frac{\text{useful } P_{out}}{\text{total generated } P_{out}} = \frac{\text{Re}\{Y_n\}}{\text{Re}\{Y_n\} + G_{D1}} = \text{output circuit effiency}$$

And so the total multiplier efficiency becomes the product of the input and output circuit efficiencies and hence, the efficiency, η, is

$$\eta = \frac{\text{Re}\{Y_{in}\} - G_{D1}}{\text{Re}\{Y_{in}\}} \; \frac{\text{Re}\{Y_n\}}{\text{Re}\{Y_n\} + G_{Dn}} \qquad (16)$$

Now Y_{in} is given in terms of the Y-parameters which will be determined in section 3.4.3 from the varactor equations of motion. However, the tuning of the multiplier will first be considered which will give rise to simplifying conditions.

3.4.2 - The Tuning Condition

This condition refers to the tuning of the input and output multiplier circuits.

From previous work done on varactor multipliers with the diode reverse-biased, ②,④ it is seen that tuning the input and output circuits with the average diode capacitance results in maximum efficiency for a given R.F. drive level. For the current pumped case of the abrupt junction varactor it is shown by Diamond ④ that the output and idler currents are all in phase with the input for all orders of multiplication.

It is further shown in reference (11) that for the quintupler all currents are in phase if the input current phase angle is arbitrarily set equal to zero, with no loss of generality. These authors ⑪ further found that to obtain maximum efficiency the circuit had to be slightly detuned. Reference (11) and (4) and also (15) all show that when the multiplier circuits are tuned all currents are in phase.

Detuning, Diamond ④ states, may increase the efficency in multiplication by about 2-3 per cent. On the other hand reference 11 says that slight detuning of an experimental tripler caused a considerable increase in efficiency whereas for the quintupler detuning had only a small effect. It is the relative current magnitudes that are very critical in high efficiency multipliers.

However, the addition of phase variables greatly complicates the theory and the simplifying tuning assumption

was made mainly for that reason in past analyses. Yet, on the other hand, it is true that detuning of the multiplier circuit would decrease the spectral output purity since these tuned circuits act as the filters for the multipliers. Thus it is doubtful whether an increase in efficiency, because of detuning, would offset the added disadvantage of poor filtering. This has been verified by the author of this thesis with experimental doublers and triplers.

This analysis of this thesis also assumes tuned conditions throughout the multiplier (see section 3.4.3). However, a more valid argument for tuning the input and output of the multiplier is the consideration of maximum power transfer. The maximum power transfer theorem for complex networks says that given a complex circuit input admittance maximum power is transferred only when the generator admittance is the complex conjugate of the input admittance. This consideration holds, of course, also for power transfer from the output of the network to a load. So that the load admittance must be the complex conjugate of the circuit output admittance. These conditions are applied in section 3.4.3.

At this point it will also be assumed that the input and output voltages are in phase on the basis of the arguments set forth in this section, realizing that the final results are subject to this assumption.

Thus $V_1 = V_1{}^*$ (by choice of time origin) (17)

and $V_n = V_n{}^*$ (by assumption)

3.4.3. - Y-Parameters from Varactor Equations of Motion Used to Determine the Multiplier Efficiency

To find the short-circuit Y-parameters of the multiplier we can expand equation (12) for the values of $k = 1, n$ in order to get the equations for I_1 and I_n. Thus assuming ideal filtering, (12) becomes,

$$I_k = (G_D + jk\omega_o C_o) V_k + \sum_{\substack{r = \pm 1, \pm n \\ r \neq k}} (jr\omega_o) C_{k-r} V_r \qquad (k \neq 0)$$

(Recall that only V_1, $V_1{}^*$, V_n and $V_n{}^*$ can exist in the multiplier). Expanding for $k = 1, n$ and remembering that G_D is frequency dependent there results,

$$I_1 = (G_{D_1} + j\omega_o C_o)V_1 + j\omega_o(-C_2 V_1{}^* - n\, C_{1+n} V_n{}^* + n\, C_{1-n} V_n)$$

$$I_n = (G_{Dn} + jn\omega_o C_o)V_n + j\omega_o(-C_{n+1} V_1{}^* - n\, C_{2n} V_n{}^* + C_{n-1} V_1)$$

Applying condition (17) yields,

$$I_1 = \left[G_{D_1} + j\omega_o(C_o - C_2)\right] V_1 + jn\omega_o(C_{1-n} - C_{1+n})V_n \tag{18a}$$

$$I_n = j\omega_o(C_{n-1} - C_{n+1})V_1 + \left[G_{Dn} + jn\omega_o(C_o - C_{2n}\right]V_n \tag{18b}$$

Comparing the coeffiecients of the V's with the Y-parameters of equation (13) gives,

$$Y_{11} = G_{D_1} + j\omega_o(C_o - C_2) \qquad Y_{1n} = jn\omega_o(C_{1-n} - C_{1+n}) \tag{19}$$

$$Y_{n1} = j\omega_o(C_{n-1} - C_{n+1}) \qquad Y_{nn} = G_{Dn} + jn\omega_o(C_o - C_{2n})$$

Now we have completely specified the nonlinear varactor behavior by means of these "nonlinear" Y-parameters of a two port with ideal filters. They are "nonlinear" because the capacitance coefficients on which they depend are a complicated function of the varactor drive level (see section 4.3).

Recall from equation (14) that the input admittance is,

$$Y_{in} = Y_{11} - \frac{Y_{1n}Y_{n1}}{Y_{nn} + Y_n}$$

Substitution of the Y-parameters of equation (19) yields,

$$Y_{in} = G_{D_1} + j\omega_o(C_o - C_2) + \frac{n\omega_o^2(C_{1-n} - C_{1+n})(C_{n-1} - C_{n+1})}{G_{Dn} + jn\omega_o(C_o - C_{2n}) + G_n + jB_n} \quad (20)$$

Similarly we obtain the output admittance by substitution of (19) into (15),

$$Y_{out} = G_{Dn} + jn\omega_o(C_o - C_{2n}) + \frac{n\omega_o^2(C_{1-n} - C_{1+n})(C_{n-1} - C_{n+1})}{G_{D_1} + j\omega_o(C_o - C_2) + G_g + jB_g} \quad (21)$$

As discussed in Section 3.4.2 we now impose the conditions that,

$Y_G = Y_{in}^*$ or, $G_g = G_{in}$ and $jB_g = -jB_{in}$ (22)

$Y_n = Y_{out}^*$ or, $G_n = G_{out}$ and $jB_n = -jB_{out}$

Then, from (20) and (21) results, using (22),

$B_g = -\omega_o(C_o - C_2) = -B_{in}$ (23)

$B_n = -n\omega_o(C_o - C_{2n}) = -B_{out}$

Then from (20) and (21) using (23) we get,

$$G_{in} = G_{D_1} + \frac{n\omega_o^2 (C_{1-n} - C_{1+n})(C_{n-1} - C_{n+1})}{G_{Dn} + G_n} \qquad (24)$$

and,

$$G_{out} = G_{Dn} + \frac{n\omega_o^2 (C_{1-n} - C_{1+n})(C_{n-1} - C_{n+1})}{G_{D_1} + G_g} \qquad (25)$$

The optimum operating conditions of the multiplier are further determined by setting, see equation (22),

$$G_{in} = G_g$$

$$G_{out} = G_n$$

Normalizing these conductances with respect to the input and output loss conductances we let,

$$X_g = G_g/G_{D_1} \qquad \text{and} \qquad X_n = G_n/G_{Dn} \qquad (26)$$

Making these substitutions in equations (24) and (25) gives the generator and load conductance for maximum power transfer, hence,

$$X_g = 1 + \frac{n\omega_o^2}{G_{D_1} G_{Dn}} \; \frac{(C_{1-n} - C_{1+n})(C_{n-1} - C_{n+1})}{1 + X_n} \qquad (27)$$

$$X_n = 1 + \frac{n\omega_o^2}{G_{D_1} G_{Dn}} \; \frac{(C_{1-n} - C_{1+n})(C_{n-1} - C_{n+1})}{1 + X_g} \qquad (28)$$

Note, however, that the generator conductance is a function of the load conductance and vice versa. So that even though equations (27) and (28) give optimum values in a sense, the true optimum for X_g is found by using the optimum value of X_n in (27) and similarly $X_{n_{opt}}$ is found by substitution of $X_{g_{opt}}$ into (28).

Doing this and defining a parameter,

$$K \equiv \frac{n\omega_o^2}{G_{D_1} G_{Dn}} (C_{1-n} - C_{1+n})(C_{n-1} - C_{n+1}) \qquad (29)$$

we get after substitution for X_n into (27),

$$X_{g_{opt}} = 1 + \cfrac{K}{2 + \cfrac{K}{1 + X_{g_{opt}}}}$$

which becomes

$$X_{g_{opt}} \left[2(1 + X_{g_{opt}}) + K \right] = 2(1 + X_{g_{opt}}) + K + K(1 + X_{g_{opt}})$$

from which,

$$X_{g_{opt}} = \sqrt{1 + K} \tag{30}$$

which thus gives us the normalized optimum generator conductance in terms of the parameter, K.

Similarly when we solve for $X_{n_{opt}}$ from (28) the result is,

$$X_{n_{opt}} = \sqrt{1 + K} \tag{31}$$

Hence, we conclude that the optimum values for X_n and X_g are equal. Recall, that since $G_{in} = G_g$ and $G_{out} = G_n$, the efficiency for multiplication can now be written by equation (16) as,

$$\eta = \frac{G_{in} - G_{D_1}}{G_{in}} \frac{G_n}{G_n + G_{Dn}} = \frac{X_{in} - 1}{X_{in}} \frac{X_n}{X_n + 1}$$

and since $X_{in} = X_{n_{opt}}$

$$\eta_{opt} = \frac{X_{n_{opt}} - 1}{X_{n_{opt}} + 1} \tag{32}$$

Since for most practical diodes the total diode loss conductance, G_D, reduces to G_s, the parallel equivalent of R_s (see section 3.2), the expression for cutoff frequency given in equation (3) along with equation (1) can be used to yield,

$$G_{D_1} = n^2 G_{Dn} = \frac{\omega_o^2 C_{min}}{\omega_c} \tag{33}$$

Substitution of (33) into(29) gives K as,

$$K = \left(\frac{\omega_c}{\omega_o}\right)^2 \frac{1}{n C_{min}^2} (C_{1-n} - C_{1+n})(C_{n-1} - C_{n+1}) \tag{34}$$

Now equations (30) and (31) can finally be written as

$$X_{g_{opt}} = X_{n_{opt}} = \sqrt{1 + \left(\frac{\omega_c}{\omega_o}\right)^2 \frac{1}{nC_{min}^2} (C_{1-n} - C_{1+n})(C_{n-1} - C_{n+1})} \tag{35}$$

and equation (32) becomes,

$$\eta_{opt} = \frac{\sqrt{1 + \left(\frac{\omega_c}{\omega_o}\right)^2 \frac{1}{nC_{min}^2} (C_{1-n} - C_{1+n})(C_{n-1} - C_{n+1})} - 1}{\sqrt{1 + \left(\frac{\omega_c}{\omega_o}\right)^2 \frac{1}{nC_{min}^2} (C_{1-n} - C_{1+n})(C_{n-1} - C_{n+1})} + 1} \tag{36}$$

This final expression gives the optimum efficiency for a large signal frequency multiplier in terms of the varactor cutoff frequency and the nonlinear capacitance coefficients which still depend on the input drive level of the diode. The only assumptions made in the derivation of this efficiency are that the varactor output and input voltages are in phase and that the loss in the diode is mainly attributed to the series diode resistance, R_s. This last assumption can easily be corrected for, if necessary, since ω_c is a direct measure of this loss. The efficiency expression holds for any varactor capacitance voltage variation when the diode is series connected in a multiplier circuit.

3.4.4 Determination of Other Important Multiplier Relationships

Besides knowing how the efficiency and the multiplier generator or load admittance depend on the frequency and drive level it is important to know the power handling capability of the multiplier.

From figure 39 it is clear that the optimum input power is given by:

$$P_{in} = \left| v_1 \right|^2 G_{in}$$

and since $G_{in} = G_{g_{opt}}$ substitution of equation (30) in the above yields,

$$P_{in} = \left| v_1 \right|^2 G_{D_1} \sqrt{1 + K}$$

where K is given by equation (34). If now equation (33) is also used to substitute for G_{D_1} the maximum power input becomes,

$$P_{in} = \left| v_1 \right|^2 \frac{\omega_o^2}{\omega_c} C_{min} \sqrt{1+K} \qquad (37)$$

Then since,

$$\eta = \frac{P_{out}}{P_{in}}$$

we obtain for the maximum power output

$$P_{out} = \eta P_{in} = \left| v_1 \right|^2 \frac{\omega_o^2}{\omega_c} C_{min} \sqrt{1 + K} \left[\frac{\sqrt{1 + K} - 1}{\sqrt{1 + K} + 1} \right] \qquad (38)$$

In chapter five more detailed relationships will be given for specific multipliers.

3.4.5 - A Check on the Theoretical Results by Applying Them to Special Cases

To check our expression for optimum efficiency, let us consider the case of an abrupt junction frequency doubler for which results are given in the literature, ②,④,⑯,⑫.

The efficiency for a doubler as given by reference 16 is,

$$\eta_{opt} = \frac{\sqrt{1 + \left(\frac{m_1}{2} \frac{\omega_c}{\omega_o}\right)^2} - 1}{\sqrt{1 + \left(\frac{m_1}{2} \frac{\omega_c}{\omega_o}\right)^2} + 1}$$

where m_1 is a normalized elastance coefficient, S_1/S_{max}, of which the dual is our, see equation (36),

$$\frac{C_{n-1} - C_{n+1}}{C_{min}}$$

assuming all C_k's to be real. This becomes for a doubler,

$$\frac{C_1 - C_3}{C_{min}} = m'$$

And so we can rewrite our equation (36) for a doubler as,

$$\eta_{opt} = \frac{\sqrt{1 + \left(\frac{m'}{2} \frac{\omega_c}{\omega_o}\right)^2} - 1}{\sqrt{1 + \left(\frac{m'}{2} \frac{\omega_c}{\omega_o}\right)^2} + 1}$$

which is identical in form to the expression in the literature, remembering, of course, that our m' may be different in value than the m_1 used in reference 16. The same reference also gives optimum values for optimum input and output resistances of the form,

$$R_{in_{opt}} = R_s \sqrt{1 + \left(\frac{m_1}{2} \frac{\omega_c}{\omega_o}\right)^2} = R_{load_{opt}}$$

From our equation (35) it is clear that the dual of the above is,

$$G_{in_{opt}} = G_{D_1} \sqrt{1 + \left(\frac{m'}{2} \frac{\omega_c}{\omega_o}\right)^2} = G_{load_{opt}}$$

the G_{D_1} being the dual equivalent of R_s. It is important to realize that when comparing this analysis with one where the varactor is current driven, that the equivalent circuits used for the multiplier in each case are also duals. To go from the one equivalent circuit to the other we must replace each of the circuit components by their equivalents. For example, a current generator must be transformed to an equivalent voltage generator, and so on.

3.5 - Normalization of Varactor Voltages and a Special Requirement on these Voltages for Different Drive Levels

Let us assume that a voltage is impressed on the diode given by:

$$V(t) = V_{DC} + V_1 \cos\omega_0 t + V_n \cos n\omega_0 t \qquad (39)$$

where V_{DC} = the D.C. bias voltage

n = order of multiplication

and where the assumption is made that $V_1 \cos\omega_0 t$ is in time phase with the output harmonic voltage, $V_n \cos n\omega_0 t$. Also let, the normalization voltage be,

$$V_0 = V_f - V_{min} \qquad (40)$$

where V_f = maximum forward voltage on the diode.

V_{min} = minimum forward (or reverse) voltage on the diode. (see figure 40)

Then from figure 40 it is clear that,

$$V_{DC} = \frac{V_f + V_{min}}{2} = \frac{V_0}{2} + V_{min} \qquad (41)$$

Therefore, the instantaneous a.c. normalized value of the varactor voltage is,

$$v(t) = \frac{V_1}{V_0} \cos\omega_0 t + \frac{V_n}{V_0} \cos\omega_0 t \leq \frac{V_f - V_{DC}}{V_f - V_{min}} = \frac{V_f - (V_0/2 + V_{min})}{V_f - V_{min}} = \frac{1}{2}$$

(Note, V_{DC} and V_{min} may be negative or positive)

Or rewriting this the condition on the magnitudes of the fundamental and n^{th} harmonic components is given as,

$$\frac{V_1}{V_0} \cos\omega_0 t + \frac{V_n}{V_0} \cos n\omega_0 t \leq \tfrac{1}{2}$$

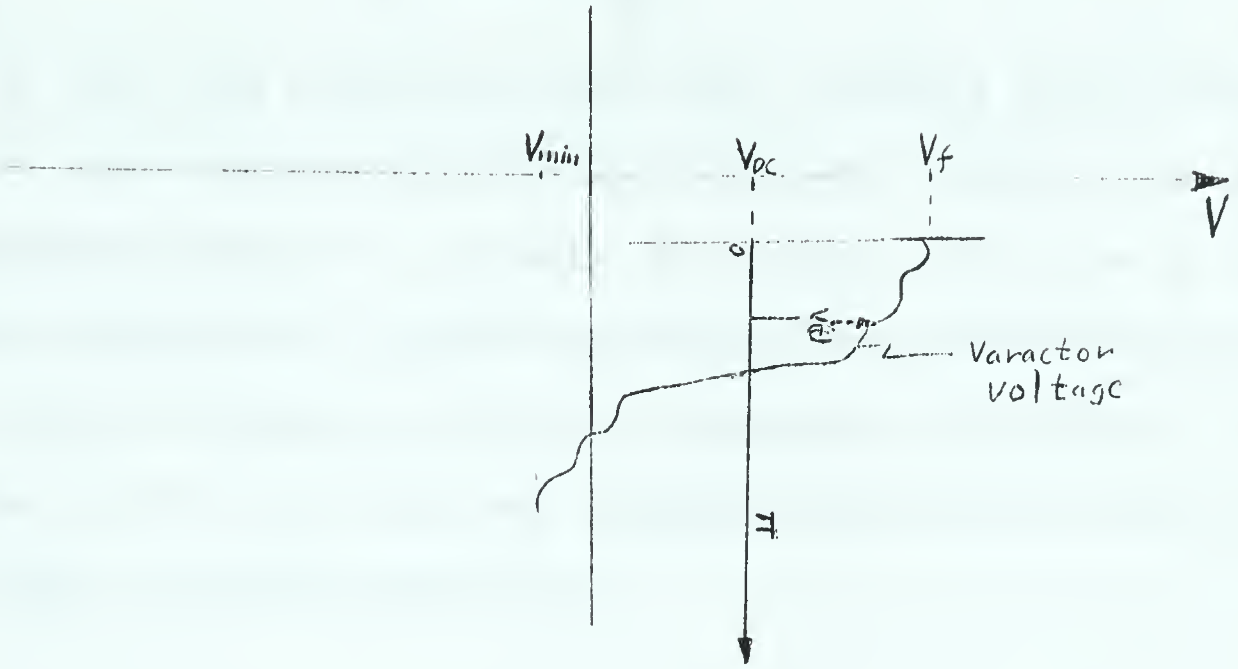


Fig. 40 Total Varactor Voltage

When condition (40) is satisfied it gives a limit on the values of V_1 and V_n for a particular drive level. For maximum voltage variation on the diode (40) becomes an equality. It seems reasonable that the varactor should be driven over its maximum voltage range since more power can be handled than when a lower drive level is used. It is also clear that this will give rise to higher efficiency since the capacitance coefficients will increase in value for higher drive levels. From now on then, condition (40) will be used with the equality sign.

Rewriting equation (42) and making the substitution $\theta = \omega_0 t$ gives,

$$\frac{V_1}{V_0} \cos\theta + \frac{V_n}{V_0} \cos n\theta = \frac{1}{2} \qquad (43)$$

It is desired to find the maximum possible values for both V_1 and V_n. It is clear from equation (43) that this maximum occurs at $\theta = 0$ and (43) becomes,

$$V_1 + V_n = \frac{V_o}{2} \qquad (44)$$

This is thus the condition which the voltages must always obey to give maximum efficiency and power output. As may be suspected there is probably an optimum value for V_1 and V_n for some specific operating conditions determined by the load, input frequency and other multiplier variables. This problem is left for the next chapter where we will try to find these optimum conditions.

CHAPTER 4

APPLICATION OF THE DERIVED THEORY TO VARACTORS WITH AN EXPONENTIAL CAPACITANCE - VOLTAGE DEPENDENCE

4.1 - Introduction

In chapter two it was already pointed out that when a multiplier is driven into the forward bias region of the diode a large increase in nonlinearity may be expected resulting in an increase in efficiency of direct harmonic generation (i.e., without the use of idler circuits). It is the primary aim of this chapter and the next to see whether this really is so for multipliers employing varactors having an exponential C-V characteristic.

As will be seen later the positive voltage excursion allowed on the varactor over this highly nonlinear characteristic is small compared to that allowed under reverse bias conditions. Nevertheless, the analysis is useful since when a diode is operated under reverse bias and "overdriven" into the positive voltage state one wants to know whether overdriving causes an increase or decrease in efficiency. On the other hand the analysis should be extremely useful for application to tunnel diode devices and circuits using MOS capacitance diodes which also have an exponential characteristic.

4.2 - The Special Charge - Voltage Relationship

A varactor biased in the forward region has an exponential dependence and the charge may be written as,

$$q(v) = A_1 \left(e^{A_2 v(t)} - 1\right) \qquad (45)$$

where,

$$A_2 = \frac{k_2 e}{KT} \text{ volt}^{-1}$$

k_2 = a constant dependent on the region of operation and on the type of varactor used (usually between $\frac{1}{2}$ and 1)

$A_1 = \frac{C_{ov}}{A_2}$

C_{ov} = capacitance at zero volts bias

Or inversely one could write,

$$v(q) = \frac{1}{A_2} \ln\left(\frac{q + A_1}{A_1}\right) \tag{46}$$

Then, the incremental capacitance is given by,

$$C(v) = \frac{dq}{dv} = \frac{d}{dv} A_1 \left(e^{A_2 v} - 1\right) = A_1 A_2 e^{A_2 v} = C_{ov} e^{A_2 v} \tag{47}$$

Using equation (45) in (47) yields,

$$C(v) = A_2 q(v) + A_1 A_2$$

Thus the capacitance is proportional to the charge on the varactor.

4.3 - Method of Determining the Capacitance Fourier Coefficients Using an Expansion for the Exponential in Terms of Modified Bessel Functions

Recall that in equation (7) the time varying capacitance function was expanded in a complex Fourier series as,

$$C(t) = \sum_{m=-\infty}^{\infty} C_m e^{jm\omega_o t}$$

It follows that,

$$C_m = \frac{1}{2\pi} \int_0^{2\pi} C(t) e^{-jm\omega_o t} d(\omega_o t) \tag{48}$$

where by equation (47),

$$C(t) = C_{ov} e^{A_2 v(t)}$$

The function v(t) is usually given as a sum of sine and/or cosine terms (see section 3.5). It is obvious that with this

complex expression for $C(t)$ the integral for C_m may be difficult to evaluate analytically.

Fortunately, for the exponential function considered here there is a method of solving for the capacitance coefficients, namely, by the use of Sonine's expansion ⑨,⑮ which is given by,

$$e^{z\cos\theta} = I_o(z) + 2\sum_{p=1}^{\infty} I_p(z)\cos p\theta \qquad (49)$$

Where $I_p(z)$ is equal to the p^{th} order modified Bessel function of the first kind with a pure imaginary argument where z is some real variable and θ can be a function of time. Thus the R.H.S. of equation (49) is in effect a Fourier series expansion of the exponential function given on the L.H.S. of equation (49). The modified Bessel functions are known functions and tabulated for many cases.

Recall that in the case of an N× multiplier only two frequency components were allowed to exist on the varactor by the proper use of filters. Thus for the n^{th} harmonic generator by equation (37),

$$v(t) = V_{DC} + V_1\cos\omega_o t + V_n\cos n\omega_o t$$

Substituting this $v(t)$ in equation (47) yields,

$$C(t) = C_{ov}\, e^{A_2(V_{DC} + V\cos\omega_o t + V_n\cos n\omega_o t)}$$

Now let $A_2V_{DC} = B_o$, $A_2V_1 = B_1$, $A_2V_n = B_n$, and $\omega_o t = \theta$. (50)

Then,

$$C(t) = C_{ov}\, e^{B_o}\, e^{B_1\cos\theta}\, e^{B_n\cos n\theta} \qquad (51)$$

(Note that the B's are dimensionless quantities since A_2 has the units of 1/volt). It is now apparent that equation (51) is of the same form as the L.H.S. of equation (49). Applying

equation (49) twice to (51) gives,

$$C(t) = C_{ov}\, e^{B_0}\left[\left(I_0(B_1) + 2\sum_{p=1}^{\infty} I_p(B_1)\cos p\theta\right)\left(I_0(B_n) + 2\sum_{r=1}^{\infty} I_r(B_n)\cos nr\theta\right)\right]$$

Designating $I_m(B_n) = I_m^n$ and expanding the above yields,

$$C(t) = C_{ov}\, e^{B_0}\Big[I_0^1 I_0^n + 2I_0^1 \sum_{r=1}^{\infty} I_r^n \cos nr\theta + 2I_0^n \sum_{p=1}^{\infty} I_p^1 \cos p\theta$$

$$+ 4\sum_{r=1}^{\infty}\sum_{p=1}^{\infty} I_r^n I_p^1 \cos nr\theta \cos p\theta\Big]$$

Using the identity,

$$\cos A \cos B = \tfrac{1}{2}\left[\cos(A+B) + \cos(A-B)\right]$$

$C(t)$ becomes,

$$C(t) = C_{ov}\, e^{B_0}\left\{I_0^1 I_0^n\right\} + \qquad (a)$$

$$+ 2C_{ov}\, e^{B_0}\left\{I_0^1 \sum_{r=1}^{\infty} I_r^n \cos nr\theta + I_0^n \sum_{p=1}^{\infty} I_p^1 \cos p\theta\right\} + \qquad (b) \qquad (52)$$

$$+ 2C_{ov}\, e^{B_0}\left\{\sum_{r=1}^{\infty}\sum_{p=1}^{\infty} I_r^n I_p^1\left[\cos(p+nr)\theta + \cos(p-nr)\theta\right]\right\} \qquad (c)$$

It is clear at this point that all the capacitance coefficients are real quantities and this means a simplification can be made in the multiplier relations derived in chapter three since now,

$$C_{1-n} = C_{n-1}^* = C_{n-1}$$

Thus the quantity,

$$(C_{1-n} - C_{1+n})(C_{n-1} - C_{n+1}) = (C_{n-1} - C_{n+1})^2 \qquad (53)$$

Thus only C_{n-1} and C_{n+1} have to be determined in order to specify the efficiency, power output, and optimum admittances of a multiplier. The coefficients C_0, C_2, and C_{2n} are needed

only to determine the magnitude of capacitative susceptance that must be tuned out in order to match the multiplier to the input and output ports. Note also, that the C_m's in this chapter are twice the value of the C_m's used in chapter three since,

$$C_m e^{jm\omega_0 t} + C_m^* e^{-jm\omega_0 t} = 2C_m \cos m\omega_0 t \qquad (54)$$

There is one difficulty, however, in evaluating equation (52). The term (52C) gives rise to an infinite series of cosine terms at any one particular frequency having different coefficients depending on the values of p and r, for there will always exist for each integer p an integer r which will give the correct frequency term, $k\theta = (p \pm n r)\theta$ ($k\theta$ being the frequency of interest), since the two sums in (52C) are independent. The magnitude of the modified Bessel functions, however, depends strongly on the argument z and the order of the function. Thus we will see that it is possible to terminate the series of $I_r I_p$ terms since the higher order $I_r I_p$ products become very small.

In order to evaluate the modified Bessel functions we must first know the magnitude of its arguments. By definition,

$B_1 = A_2 V_1$, $\qquad$ $B_n = A_2 V_n$

Further from equation (45),

$$A_2 = \frac{k_2 e}{KT}$$

or,

$A_2 = 40\ k_2$ at room termperature

$k_2 = 3/4$ to a good approximation for the forward voltage region of varactor and MOS diodes (see reference 7,

6, 19).

Thus at room temperature,

$$A_2 = 30 \tag{55}$$

Furthermore, Sah ⑲ indicates that the exponential capacitance behavior starts at a forward voltage of about 20 KT/e and goes up to about 30 KT/e, so that the range of voltage, v, is from about 500-750 millivolts. Therefore, the total voltage swing allowed on the diode will be about 250 mvolts. This is, indeed, much smaller than the voltage allowed on the diode in the reverse biased state but since the nonlinearity over this small voltage range is large it will be an important factor in determining the effect on efficiency of multiplication for an "overdriven" varactor.

In the following calculations we will assume the varactor is driven over the maximum voltage range where the exponential C-V characteristic is displayed. The complex dependence of all multiplier parameters on drive level does not warrant the detailed calculations to be carried out for all values of drive level. From the above we then have by equation (40),

$$V_o = V_f - V_{min} = 250 \text{ mvolts} \tag{56}$$

and by equation (44),

$$V_1 + V_n = 125 \text{ mvolts} \tag{57}$$

The remainder of this chapter will be devoted to the calculation of the term $(C_{n-1} - C_{n+1})$ which is the controlling factor in determining the multiplier efficiency. In order to arrive at a value for this term the multiplication factor, n, must of necessity be specified. Since we are interested in

the maximum efficiency it is also necessary to arrive at some optimum value for V_1 and V_n, the magnitudes of the input and output voltage. These problems will now be dealt with.

4.4 - Capacitance Coefficients for a Doubler with Maximum Drive

In the case of a doubler, the multiplication factor n is equal to 2. In equation (52) only the (b) and (c) terms will contribute to the a.c. capacitance coefficients. We proceed to find the values for the most important capacitance factor namely, $(C_{n-1} - C_{n+1})$. Expanding equation (52b) for $n = 2$,

$$2C_{ov}e^{B_0}\Big[I_0^2 I_1^1 \cos\theta + \left(I_0^1 I_1^2 + I_0^2 I_2^1\right)\cos 2\theta + \qquad (58)$$

$$+ I_0^2 I_3^1 \cos 3\theta \quad + \left(I_0^1 I_2^2 + I_0^2 I_4^1 \cos 4\theta\right) + \cdots \Big]$$

Now for a doubler $(C_{n-1} - C_{n+1}) = C_1 - C_3$ and hence the contribution from (52b), denoted by $(C_1 - C_3)^b$; is,

$$(C_1 - C_3)^b = 2C_{ov}e^{B_0} I_0(B_2)\left[I_1(B_1) - I_3(B_1)\right] \qquad (59)$$

which reduces by the use of the identity,

$$I_{n-1}(Z) - I_{n+1}(Z) = \frac{2n\, I_n(Z)}{Z} \qquad (60)$$

to,

$$(C_1 - C_3)^b = \frac{8\, C_{ov}\, e^{B_0}\, I_0(B_2) I_2(B_1)}{B_1} \qquad (61)$$

From equation (52c) we also get an important contribution to the $(C_1 - C_3)$ factor. This is denoted by $(C_1 - C_3)^c$. Rewriting equation (52c), for $n = 2$, gives,

$$2\,C_{ov}\,e^{B_0}\sum_{p=1}^{\infty}\sum_{r=1}^{\infty} I_r^{2} I_p^{1}\left[\cos(p+2r)\theta + \cos(p-2r)\theta\right] \tag{62}$$

For the terms of interest we set,

$$p + 2r = \pm 1 \quad (\text{for the } \cos\theta \text{ terms})$$

(remebering that $\cos(-\theta) = \cos\theta$)

Thus, $$r = \frac{\pm 1 - p}{2} \tag{63}$$

and no contribution to the $\cos\theta$ terms can come from this combination since both r and p must be positive integers.

Also, $$p + 2r = \pm 3 \quad (+ \cos 3\theta \text{ contribution})$$

hence, $$r = \frac{\pm 3 - p}{2} \tag{64}$$

which gives $r = 1$ and $p = 1$ as the only possible values for this relation. Further,

$$p - 2r = \pm 1 \quad (+ \cos\theta \text{ contribution})$$

which gives,

$$r = \frac{p \pm 1}{2} \tag{65}$$

And contributions to the $\cos\theta$ term result for odd values of p only, i.e., $r = 1,2,3,\ldots$ for $p = 1,3,5,7,\ldots$

Finally, we set,

$$p - 2r = \pm 3 \quad (+ \cos 3\theta \text{ contribution})$$

from which,

$$r = \frac{p \pm 3}{2} \tag{66}$$

where again $r = 1,2,3,\ldots$ for $p = 1,3,5,7,\ldots$

Using equations (63), (64), (65), and (66) in (62) yields,

$$(C_1 - C_3)^c = 2\,C_{ov}\,e^{B_0}\left[\sum_{\substack{p=1\\ odd}}^{\infty} I^2_{\frac{p\pm1}{2}} I_p^1 - \left(I_1^2 I_1^1 + \sum_{\substack{p=1\\ odd}}^{\infty} I^2_{\frac{p\pm3}{2}} I_p^1\right)\right] \tag{67}$$

where $p \pm m/2$ must always be a positive integer greater than zero. Most of the higher order terms in equation (67) can be neglected for the range of arguments used here. The total capacitance factor $(C_1 - C_3)$ is now simply obtained by adding equation (61) and (67) and hence the $(C_{n-1} - C_{n+1})$ factor for a doubler is known from which all the important multiplier parameters can be determined.

Equation (61) and (67) will now be evaluated for the maximum range of the arguments, B_1 and B_2. By use of equation (50) and (57) the condition on B_2 and B_1 is found to be,

$$B_1 + B_2 = 3.75 \tag{68}$$

This condition when satisfied will insure that the capacitance diode is driven over its full useable range where it exhibits the exponential voltage dependence. This will in turn give rise to conditions on the input and output admittances of the multiplier circuit (see chapter 5). All that remains to be done in this section is to obtain a plot of equation (61) plus (67) versus B_1 or V_1. This is done in figure 41 where only the largest terms in equation (67) were used. The $(C_1 - C_3)^c$ term was calculated from equation (66) to be,

$$(C_1 - C_3)^c = 2C_{ov}e^{B_0}\left[-I_2^2(I_1' - I_3') - I_3'I_3^2 + I_1^2(I_3' - I_5')\right] \tag{69}$$

where the higher order terms were found to be negligible. On figure 41 the $(C_1 - C_3)$ factor is normalized with respect to $2C_{ov}\,e^{B_o}$.

4.5 - Capacitance Coefficients for a Triper With Maximum Drive

The procedure here is much the same as that used in

section 4.4 and hence only the main results are indicated here. Using n = 3 in equation (52b) gives,

$$2C_{ov}\,e^{Bo}\Big[I_0^3 I_1^1 \cos 3\theta + I_0^3 I_2^1 \cos 2\theta + (I_0^3 I_3 + I_1^3 I_0^1)\cos 3\theta + I_0^3 I_4^1 \cos 4\theta + \dots\Big] \tag{70}$$

The $C_{n-1} - C_{n+1}$ term for a tripler becomes $(C_2 - C_4)$ and,

$$(C_2 - C_4)^b = 2C_{ov}e^{B_0} I_0(B_3)\left[I_2(B_1) - I_4(B_1)\right]$$

which reduces by equation (60) to,

$$(C_2 - C_4)^b = \frac{12C_{ov}e^{B_0}}{B_1} I_0(B_3) I_3(B_1) \tag{71}$$

This is the contribution of the (52b) term to the $(C_{n-1} - C_{n+1})$ factor for the tripler. From equation (52c) results,

$$2C_{ov}e^{B_0}\sum_{r=1}^{\infty}\sum_{p=1}^{\infty} I_r^3 I_p^1\left[\cos(p+3r)\theta + \cos(p-3r)\theta\right] \tag{72}$$

For the terms of interest we set,

$$p + 3r = \pm 2, \pm 4 \quad \text{and } p - 3r = \pm 2, \pm 4 \tag{73}$$

Substituting into equation (72) and collecting terms yields,

$$(C_2 - C_4)^c = 2C_{ov}e^{B_0}\left[-I_1^1 I_1^3 + \sum_{p=1}^{\infty} I^3_{\frac{p\pm 2}{3}} I_p^1 - \sum_{p=2}^{\infty} I^3_{\frac{p\pm 4}{3}} I_p^1\right] \tag{74}$$

where $(p \pm m)/3$ must be a positive integer greater than zero. The terms contributing to $(C_2 - C_4)^c$ are then given by,

$$(C_2 - C_4)^c = 2C_{ov}e^{B_0}\left[-I_2^3(I_2^1 - I_4^1) + I_5^1(I_1^3 - I_3^3)\right] \tag{75}$$

where again the higher order terms are negligible. The sum of equation (75) and (71) is plotted versus V_1 in figure 41 subject to the condition

$$B_1 + B_3 = 3.75$$

The next chapter will deal with particular characteristics of the doubler and tripler discussed here. Optimum values for the $(C_{n-1} - C_{n+1})$ factor will have to be found for various

frequencies from which efficiency and load admittance can then be plotted as functions of multiplier frequency.

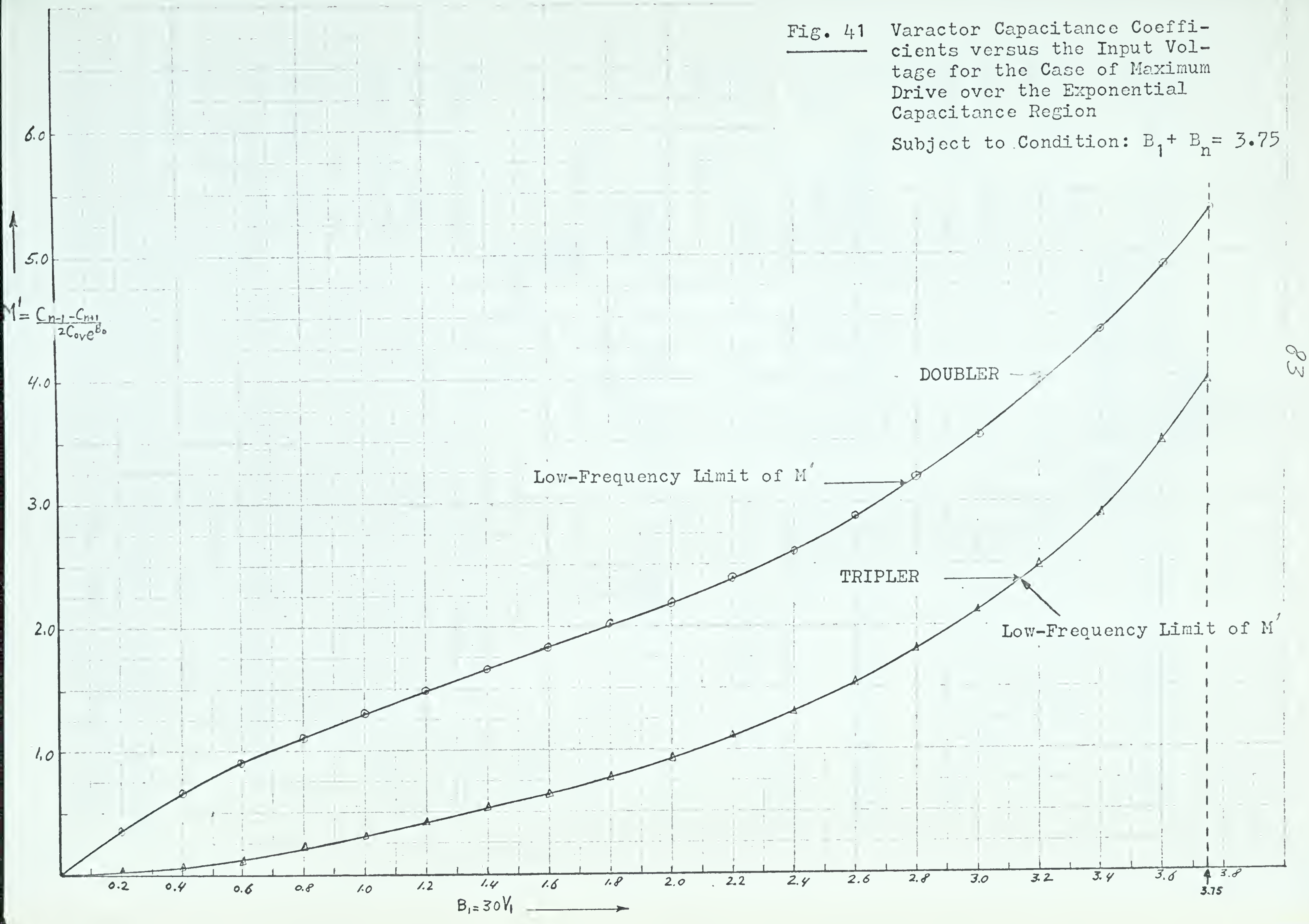


Fig. 41 Varactor Capacitance Coefficients versus the Input Voltage for the Case of Maximum Drive over the Exponential Capacitance Region

Subject to Condition: $B_1 + B_n = 3.75$

CHAPTER 5

THEORETICAL RESULTS FOR A DOUBLER AND TRIPLER OPERATING OVER THE EXPONENTIAL REGION

It is the purpose of this chapter to present some important theoretical curves for a doubler and a tripler for which the varactor has an exponential capacitance-voltage dependence, and to interpret these curves with respect to the case of the "overdriven" varactor multiplier.

5.1 - Optimization Procedure for the Multiplier Characteristics

5.1.1 - Summary of Multiplier Relationships

From chapter three we recall that the following relations hold for a general N-times multiplier (see equations (34), (35), (36),)

$$K = \left(\frac{\omega_c}{\omega_o}\right)^2 \frac{1}{n} \left(\frac{C_{n-1} - C_{n+1}}{C_{min}}\right)^2 \equiv \left(\frac{\omega_c}{\omega_o}\right)^2 \frac{1}{n} M^2 \qquad (76)$$

$$X_{n_{opt}} = \frac{G_n}{G_{Dn}} = \sqrt{1 - K} \qquad (77)$$

$$\eta_{opt} = \frac{\sqrt{1 + K} - 1}{\sqrt{1 + K} + 1} \qquad (78)$$

Where equations (77) and (78) give optimum values for X_n and η with respect to maximum power output since in chapter three these equations were derived under the condition of maximum power transfer. Efficiency and load conductance are both strongly dependent on the voltage existing on the diode. To find the optimum value of drive level we must find another relationship between the varactor voltages and the load admittance on capacitance coefficients. Such a relation can be found from the general two port multiplier network discussed in chapter three. The magnitude of the input to output ratio

is then given by,

$$\left|\frac{V_n}{V_1}\right| = \frac{|Y_{n1}|}{|Y_{nn} + Y_n|} \tag{79}$$

which by the use of equation (19) becomes,

$$\left|\frac{V_n}{V_1}\right| = \frac{\omega_o(C_{n-1} - C_{n+1})}{G_n + G_{Dn}}$$

By the use of equations (26) and (33) the above expression yields,

$$\left|\frac{V_n}{V_1}\right| = \frac{\omega_c}{\omega_o} \frac{1}{n^2 C_{min}} \frac{(C_{n-1} - C_{n+1})}{X_n + 1}$$

Finally substitution of equation (76) in this expression gives,

$$\left|\frac{V_n}{V_1}\right| = \frac{\sqrt{\frac{K}{n^3}}}{X_n + 1} \tag{80}$$

The cutoff frequency, ω_c, defined by equation (3) will of course be different for a reverse biased than for a forward biased diode because of its dependence on C_{min} which is the minimum capacitance over the operating region of the diode. In order that the results of this chapter can be interpreted in terms of the ω_c specified by varactor manufacturers, based on the capacitance at the reverse breakdown voltage, a conversion factor has to be found to make the K-parameter of equation (76) calculable in terms of known quantities.

Let F and B denote the forward and reverse bias case respectively. Then by equation (3) we obtain,

$$\frac{\omega_{cF}}{\omega_{cB}} = \frac{C_{min\,B}}{C_{minF}} \quad \text{(assuming } R_s \text{ the same for both cases)}$$

or,

$$\omega_{cF} = \frac{C_{minB}}{C_{minF}} \omega_{cB} \tag{81}$$

Further, from equation (76) the parameter M is,

$$M = \frac{C_{n-1} - C_{n+1}}{C_{minF}}$$

The C_m's here are the Fourier coefficients of the complex $e^{jm\omega t}$ terms as originally defined in chapter three. However, in chapter four the C_m's were the coefficients of cos $m\omega t$ terms. It is clear that

$$C_m e^{jm\omega t} + C_m^* e^{-jm\omega t} = 2\left|C_m\right| \cos m\omega t = C_m' \cos m\omega t$$

and hence,

$$C_m = \frac{C_m'}{2} \tag{82}$$

The value plotted in figure 41 for the doubler and tripler is,

$$M' = \frac{C_{n-1}' - C_{n+1}'}{2C_{minF}\, e^{Bo}} \tag{83}$$

Since $C_{ov} = C_{minF}$, where the subscript "ov" refers to the point where the exponential capacitance behavior starts. Using equations (81), (82), and (83) in equation (76) results in,

$$K = \left(\frac{\omega_{cB}}{\omega_o}\right)^2 \frac{1}{n} \left(\frac{C_{minB}}{C_{minF}}\right)^2 \left(\frac{C_{n-1}' - C_{n+1}'}{2C_{minF}\, e^{Bo}}\right)^2 e^{2Bo} \tag{84}$$

Now for typical varactors,

$$C_{minB} \cong \frac{C_{minF}}{50}$$

This value is assumed only in order to compare our results directly with results from analyses given for reverse biased diodes. For the case of maximum excursion of the exponential region the value of D.C. bias is given by,

$$Bo = A_2 V_{DC} = 3.75$$

Then the conversion factor,

$$F = \left(\frac{C_{minB}}{C_{minF}}\right)^2 e^{2Bo} \qquad (a) \qquad (85)$$

becomes,

$$F = \frac{e^{7.5}}{(50)^2} \cong \frac{3}{4} \qquad (b)$$

And so the expression for K to be used for the computation of results is given, by substitution of equations (83) (85a) (85b) into (84), as,

$$K = \left(\frac{\omega_c}{\omega_o}\right)^2 \frac{3}{4n} M'^2 \qquad (86)$$

where ω_c now is the cutoff frequency based on C_{min} at reverse breakdown voltage, n is the order of multiplication, and M' is the normalized capacitance coefficient term given in figure 41 and defined by equation (83).

5.1.2 - Outline of Optimization Procedure

In chapter four the capacitance coefficients of most importance were calculated and plotted as a function of input voltage in figure 41. This plot is of prime importance in determining the optimum operating points for the multiplier at different frequencies. A short outline of the optimization procedure used will now be presented and will be followed by a numerical sample calculation. It is clear that optimization is necessary since all the important multiplier relations depend strongly on the drive level.

Choosing a value for the parameter K, a value for X_{nopt} can be calculated from equation (77) and the efficiency, η_{opt}, can be determined from equation (78). Using the

obtained value for $X_{n_{opt}}$ and the assumed value for K in equation (80) yields a value for the voltage ratio $\left|\frac{V_n}{V_1}\right|, \left(\left|\frac{V_n}{V_1}\right| = \left|\frac{B_n}{B_1}\right|\right)$. Then by the use of condition (57) a value for V_1 or B_1 can be obtained, Using this V_1 or B_1 the plot of M' versus B_1 in figure 41 then determines the value of M' to be used in equation (87) and from this equation the correct value for $\frac{\omega_o}{\omega_c}$ can be calculated which then corresponds to the optimum value of efficiency obtained earlier. In this manner the first point on the optimum efficiency versus normalized frequency curve is determined. This set of calculations is then repeated for a complete range of K values to give the entire curve of optimum efficiency versus normalized frequency as shown in figure 42.

This procedure is straight forward but tedious. However, if many more higher order multipliers were to be analyzed this way a computer program for these calculations would be worthwhile.

5.1.3 - Numerical Example of Optimization Procedure

A sample calculation will now be given for obtaining the optimum efficiency for some specific frequency. The example will be done for the case of a tripler, thus $n = 3$.

First a value of K is chosen, let say, $K = 50$. By equation (77) x_{opt} is immediately determined to be,

$$x_{opt} = \sqrt{1 + 50} = 7.14$$

Similarly, by equation (78) we obtain for the optimum efficiency,

$$\eta_{opt} = \frac{\sqrt{51} - 1}{\sqrt{51} + 1} = \frac{6.14}{8.14} = 75.5\%$$

Further, substituting K = 50, and $x_{opt} = 7.14$ into equation (80) yields,

$$\left|\frac{V_n}{V_1}\right| = \frac{\sqrt{\frac{50}{27}}}{8.14} = .167 = \frac{B_n}{B_1}$$

By the condition $B_n + B_1 = 3.75$ we solve for B_1 and so,

$$1.167\, B_1 = 3.75$$

$$B_1 = 3.21$$

Now going to figure 41 we enter the graph at $B_1 = 3.21$ and find the value for M' to be, $M' = 2.49$

From equation (86) we solve for $\frac{\omega_o}{\omega_c}$ and get,

$$\frac{\omega_o}{\omega_c} = \sqrt{\frac{3}{4nK}}\,(M')$$

$$\frac{\omega_o}{\omega_c} = \sqrt{\frac{3}{12 \times 50}}\,(2.49) = 1.76 \times 10^{-1}$$

and thus, $\eta_{opt} = 75.5\%$ for $\frac{\omega_o}{\omega_c} = 1.76 \times 10^{-1}$

5.2 - Evaluation of Theoretical Results Compared to Experimental Results Reported in the Literature

The optimum multiplier efficiency is given as a function of normalized frequency in figures 42 and 43 for both the doubler and the tripler. Figure 43 shows the asymptotic behavior more clearly at very low and very high input frequency. Figure 42 is plotted on probability paper to accentuate the low and high efficiencies. For comparison the maximum efficiency curve calculated by B.L. Diamond④ for an abrupt junction varactor doubler is also shown in figure 42. It is clear then that to achieve one particular efficiency the doubler using an exponential characteristic can be operated

at an input frequency which is about one order of magnitude higher than the comparable abrupt junction doubler. The tripler shown gives a somewhat lower efficiency as would be expected. The higher efficiency result , however, does not indicate that a multiplier using a varactor with strictly an exponential characteristic is superior in all respects to, for example, an abrupt junction varactor multiplier. The exponential device can handle only relatively small amounts of power as compared to a similar abrupt junction device because of its smaller voltage range. Nevertheless, the results definitely bear out the fact that an "overdriven" varactor does not necessarily have a degrading effect on the total efficiency of the multiplier. By "overdriving" we understand the following: When the voltage swing on the varactor is primarily over the reverse-biased diode region but the peaks of the voltage swing drive the diode into the forward voltage region then the varactor is said to be "overdriven".

It has been argued in the past that the diode Q falls off rapidly in the forward region and thus multiplication efficiency can be expected to decrease. However, eventhough the diode Q decreases rapidly there is simultaneously a large increase in capacitance-voltage nonlinearity which causes a large increase in harmonic content of the diode waveform. The latter effect seems to be stronger than the effect of a decreasing quality factor as shown by this analysis.

Experimental proof, that driving the varactor into the forward bias region causes a total efficiency increase has been indicated by B.L. Diamond ④ and D.B. Leeson ③. Diamond reports a quadrupler for which the efficiency was calculated to the 70%. Including circuit losses the device operated under strictly reverse bias at an efficiency of about 60%. When the varactor was overdriven considerably an increase of total multiplier efficiency to 75% was observed. This quadrupler was designed with an idler at $2\omega_0$.

Leeson reports a similar phenomena. He discusses a quintupler (X5) which gave an efficiency between 20 and 44% depending on how sharp the nonlinearity of the diode was in the forward bias region. The higher efficiency occurred for the case where diode capacitance increased the fastest for a given voltage change in the forward voltage region. His circuit did not include any idlers. Reference 13 also indicates that "overdriving" the varactor results in better overall multiplier performance.

From the results derived in this thesis it seems that a large portion of the increase in efficiencies reported can be ascribed to the exponential capacitance increase under forward bias.

Furthermore it is noted that the frequency behavior of all multiplier variables such as, input and load conductance (see figure 44), the drive parameter M' (see figure 45), and the input and output power, is very similar to the behavior

reported for other C-V characteristics. This was anticipated already in chapter three where the general multiplier equations were very similar to those derived in the literature for specific diode characteristics.

The only basic assumption made in this analysis is that the input and output voltages are in phase. This assumption was made mainly for simplifying the theory which would become prohibitively complex with the inclusion of phase variables. It may thus be possible to achieve more favorable voltage and current magnitudes by having specific phase relationships between them. However, as shown for the exponential capacitance case, the efficiency at the lower frequencies is already so high that a small increase due to more favorable voltage magnitudes is not worth the added complexity in analysis. At the higher frequencies the output voltage becomes very small with respect to the input voltage and any phase relationship between them would have little effect on the ratio of their magnitudes and thus on the high frequency efficiency.

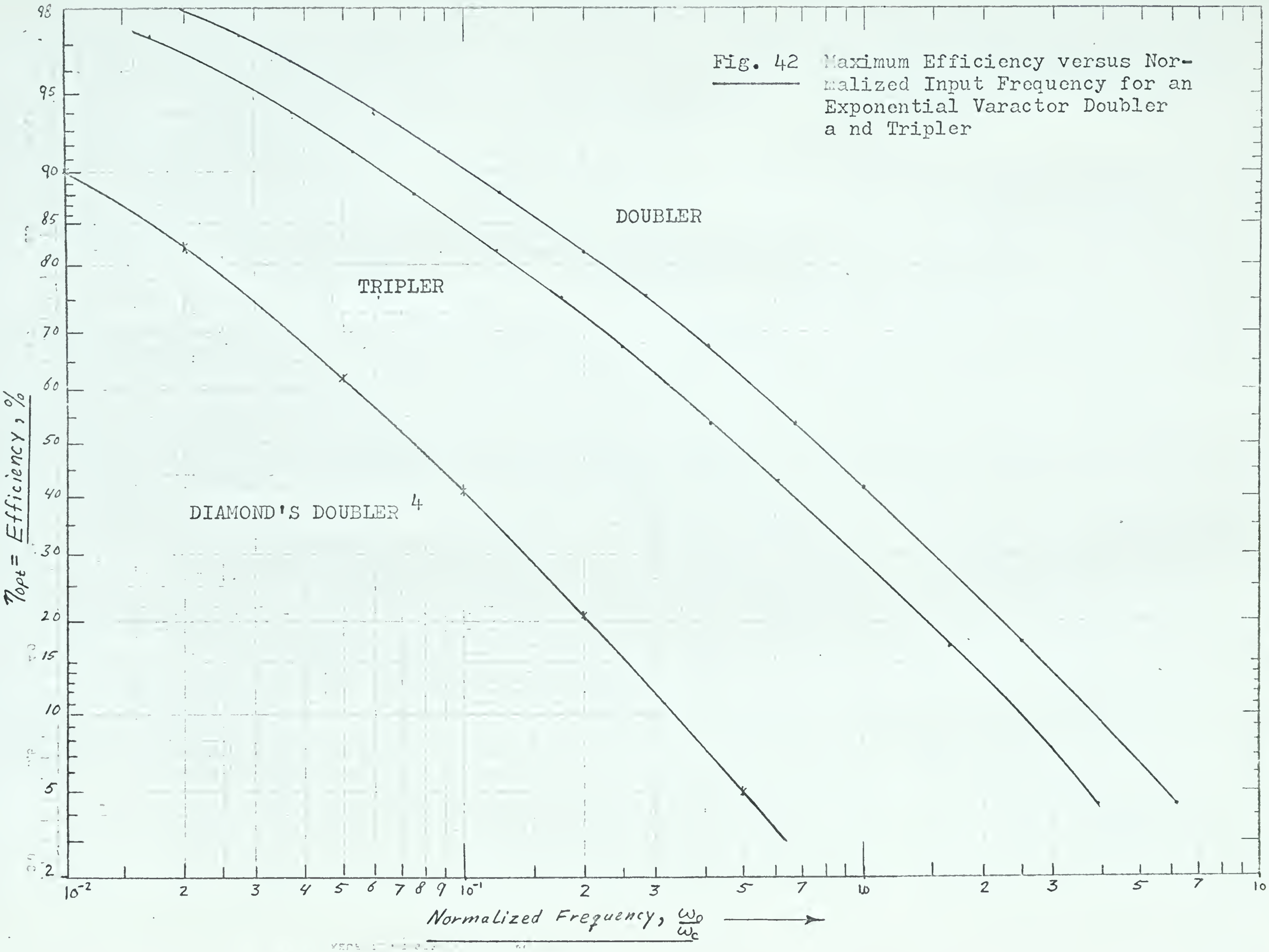
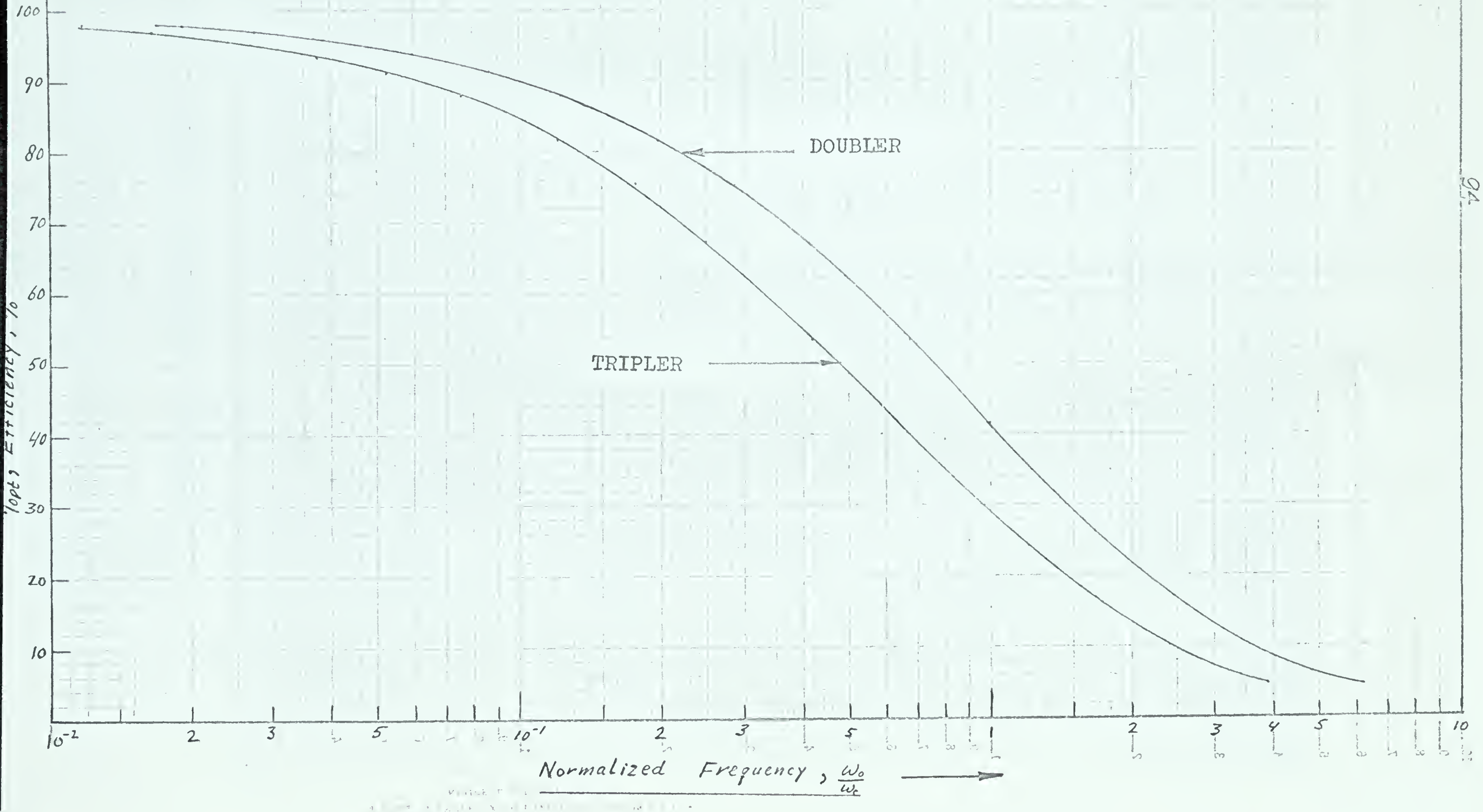


Fig. 42 Maximum Efficiency versus Normalized Input Frequency for an Exponential Varactor Doubler a nd Tripler

Fig. 43 Maximum Efficiency versus Normalized Input Frequency for an Exponentia l Varactor Doubler and Tripler



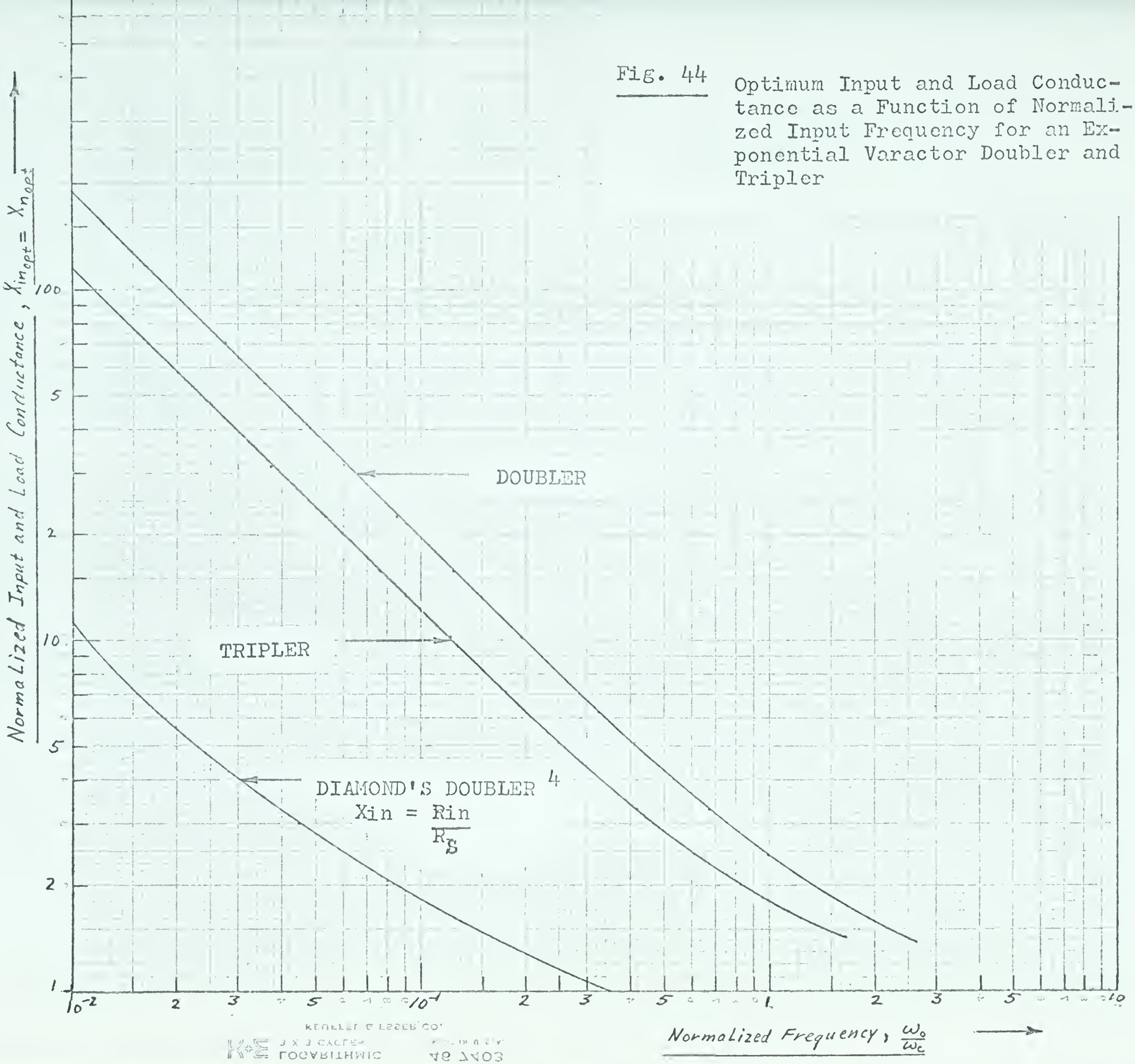


Fig. 44 Optimum Input and Load Conductance as a Function of Normalized Input Frequency for an Exponential Varactor Doubler and Tripler

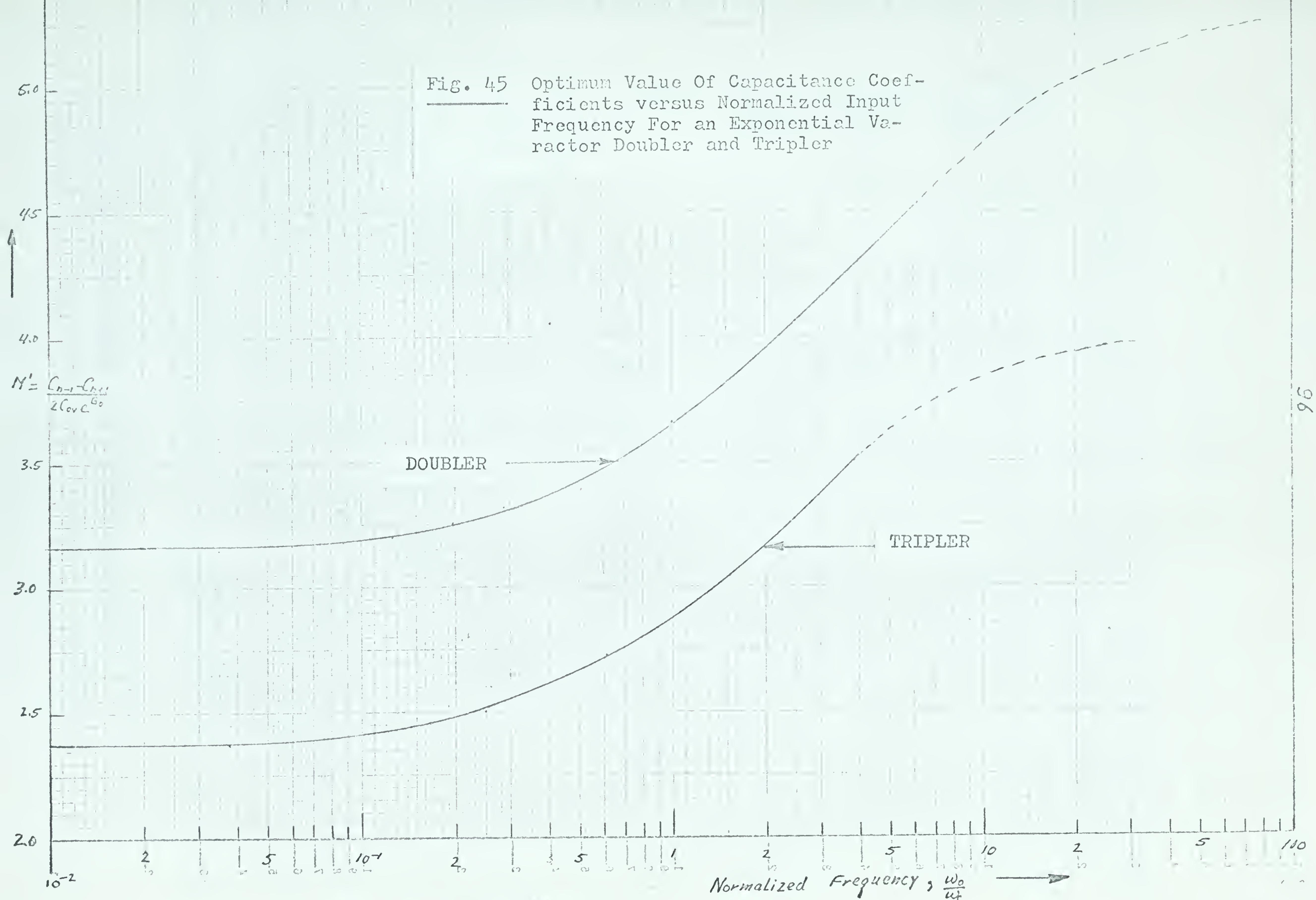


Fig. 45 Optimum Value Of Capacitance Coefficients versus Normalized Input Frequency For an Exponential Varactor Doubler and Tripler

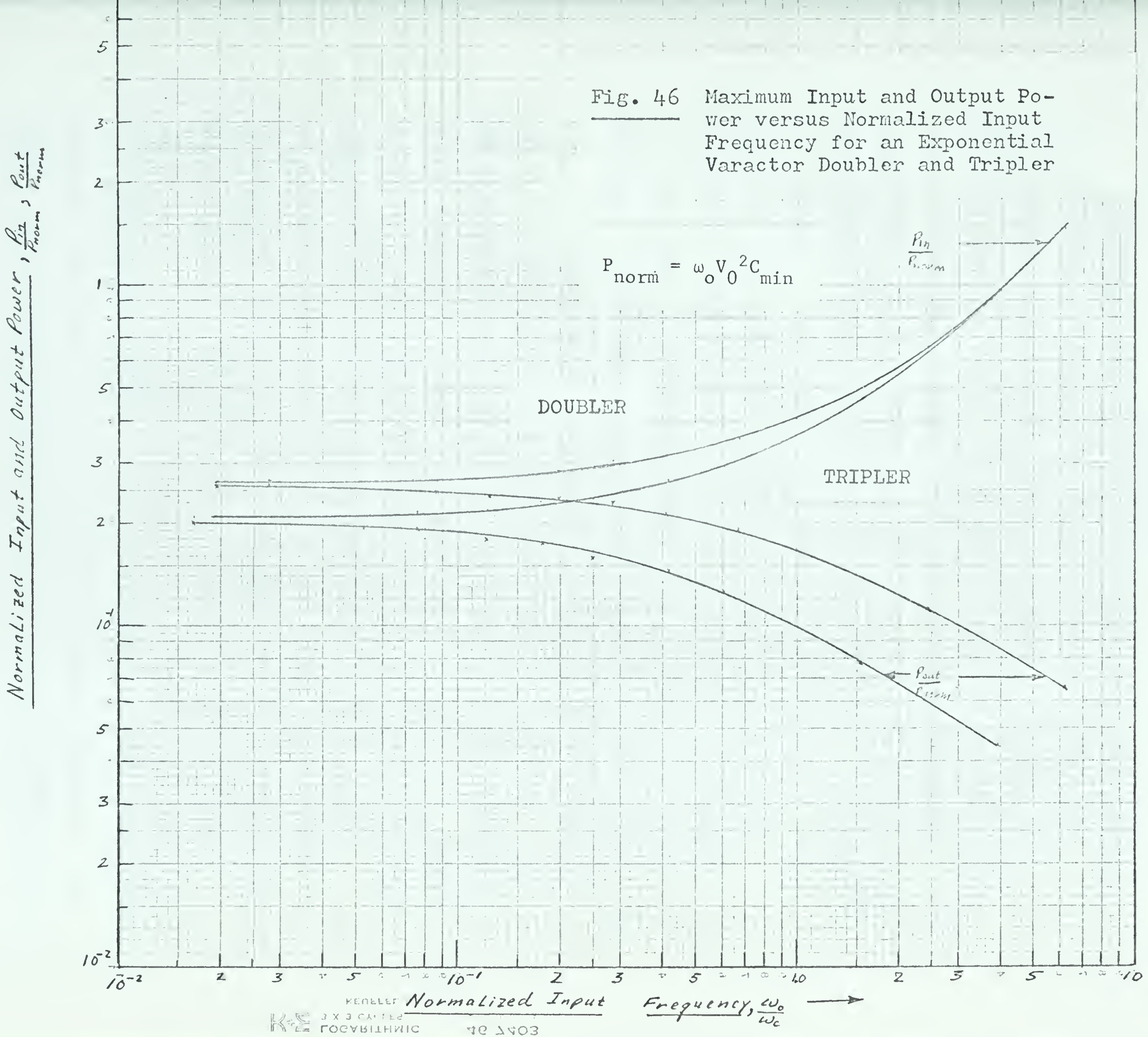


Fig. 46 Maximum Input and Output Power versus Normalized Input Frequency for an Exponential Varactor Doubler and Tripler

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CHAPTER 6

CONCLUSION

A general frequency multiplier analysis has been presented which determines completely the behavior of multipliers using varactors with a general capacitance-voltage characteristic. All that is require to apply this theory to any particular varactor is the determination of the capacitance Fourier coefficients which for many of the simpler C-V characteristics is fairly straightforward. The varactor is assumed to be series connected between input and output ports of the imbedding network. The only restrictive assumption made is that the input and output voltages are in time phase on grounds of making the problem tractable for analysis. This assumption, as discussed in section 3.4.2 and 5.2, is a reasonable one since addition of phase variables would not be expected to modify the results greatly. For maximum efficiency a definite condition is imposed on the total varactor voltage as discussed in section 3.5. Application of the derived theory to an exponential capacitance-voltage characteristic is made in chapter four and five. This exponential behavior is found to occur when the varactor is "overdriven" into the forward voltage region at frequencies high enough to insure failure of the diode rectification mechanism. It is shown that the efficiency of multiplication is considerably higher for such a highly nonlinear capacitance behavior than for the more gentle nonlinearities occurring under reverse bias operation if direct harmonic generation is

considered, i.e., in absence of idler circuits. Thus it is concluded that the combination of operating a varactor over the reverse bias region and partly over the forward voltage region will result in an enhancement of multiplier efficiency assuming, of course, that the frequency of operation is such as to allow the exponential capacitance behavior to exist for small forward biases.

Moreover, it may be interesting to see what happens when the order of multiplication goes up considerably. By comparison of the doubler and tripler curves in chapter five we would suspect that high efficiencies would result for orders of multiplication considerably larger than $n=3$, and thus overall multiplier efficiency may be expected to be enhanced even for large orders of multiplication.

With addition of this analysis the varactor frequency multiplier behavior can be specified more completely under various operating conditions. Further application of this theory can be made to other exponential devices such as tunnel diodes and surface-charge varactors. One disadvantage of the exponential behavior is that it is very temperature sensitive. However, compensation techniques could possibly be used to reduce this unwanted effect for tunnel diode and similar devices.

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